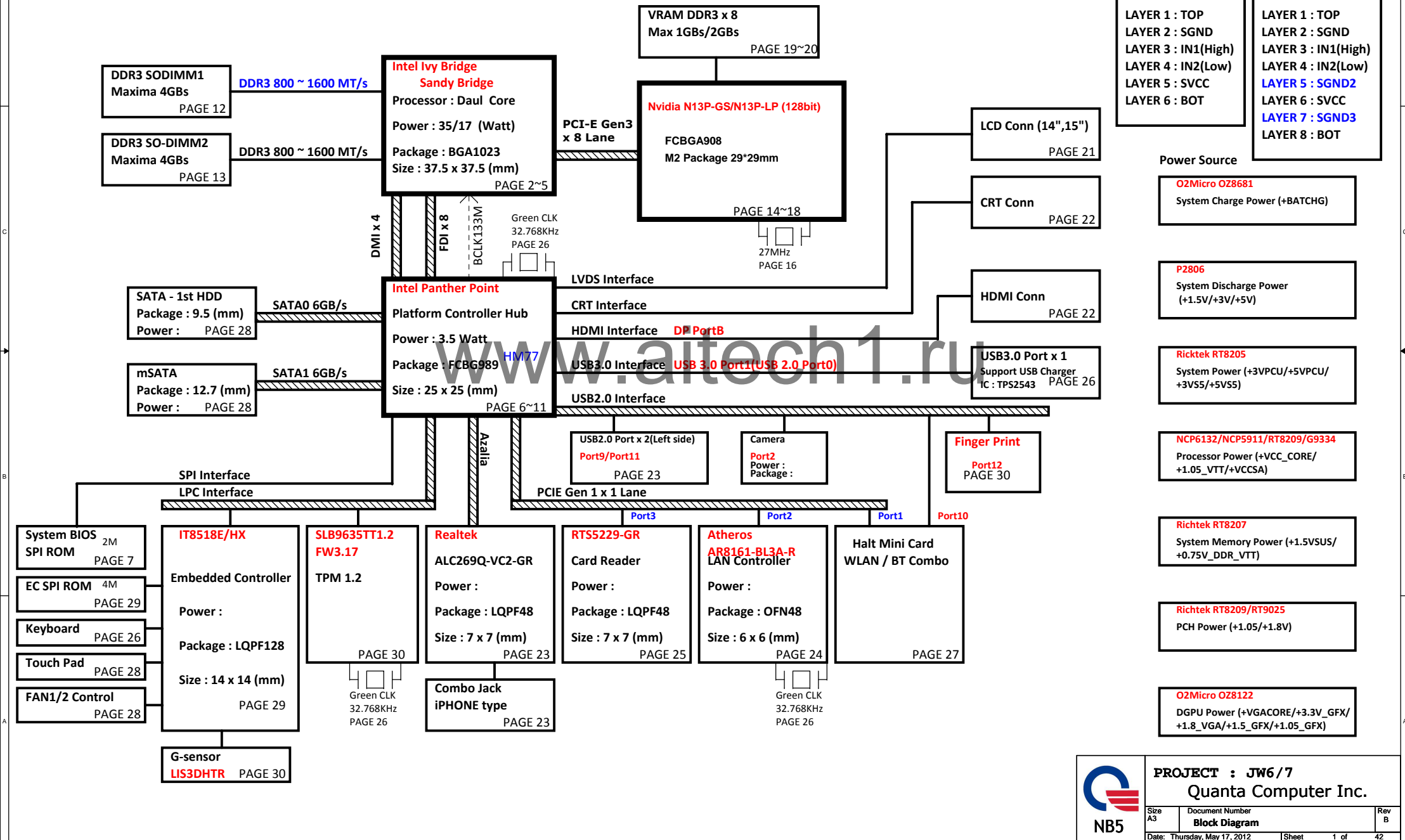
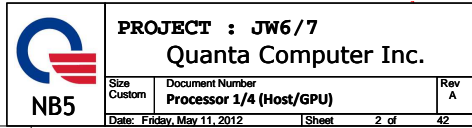
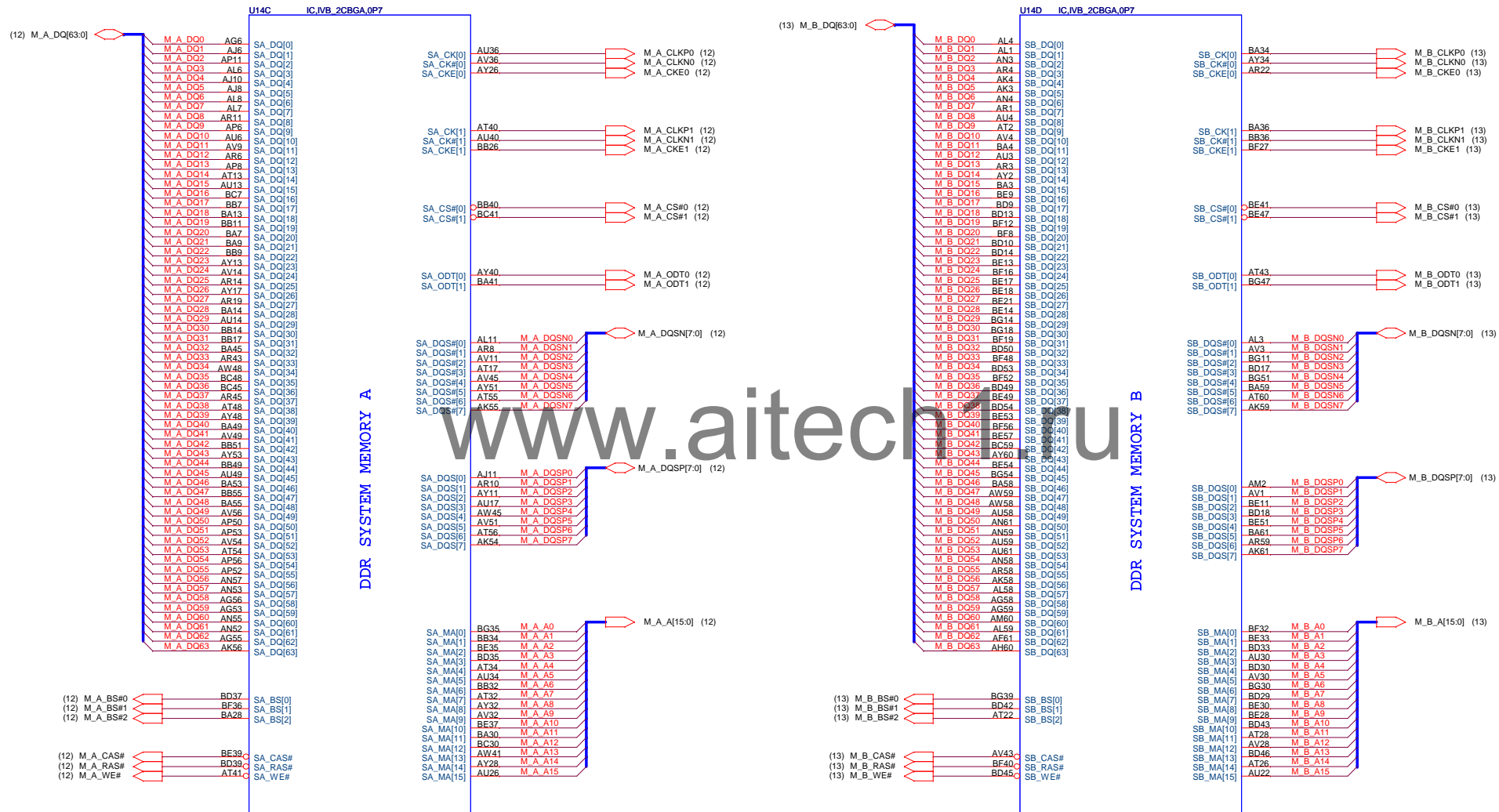


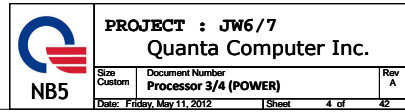
JW6/7 DIS/UMA (14",15") Ultra Intel Chief River Platform Block Diagram

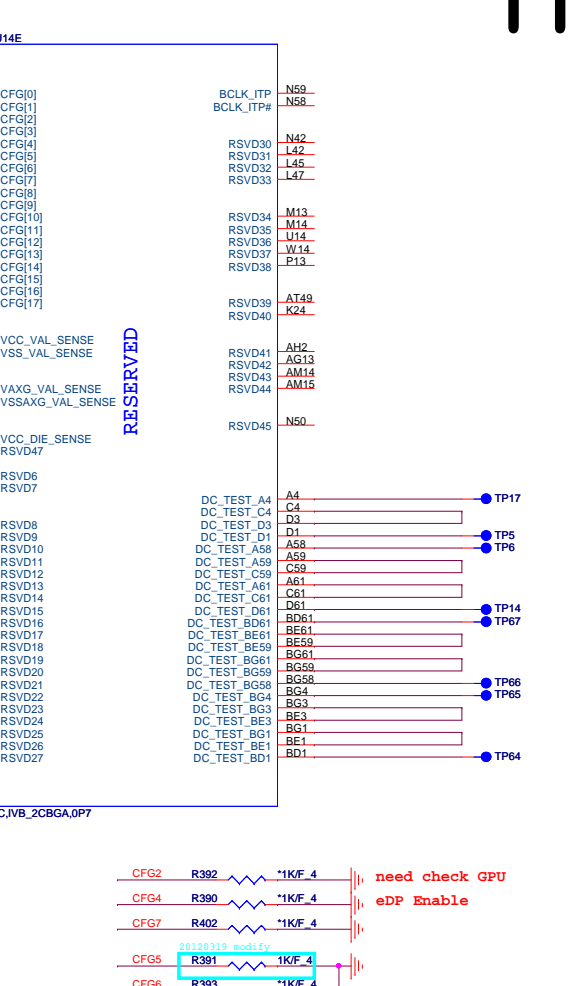
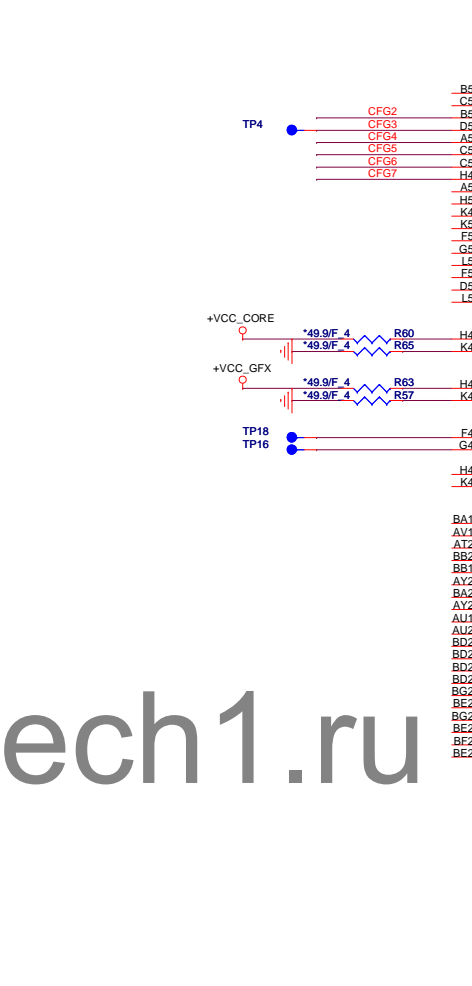
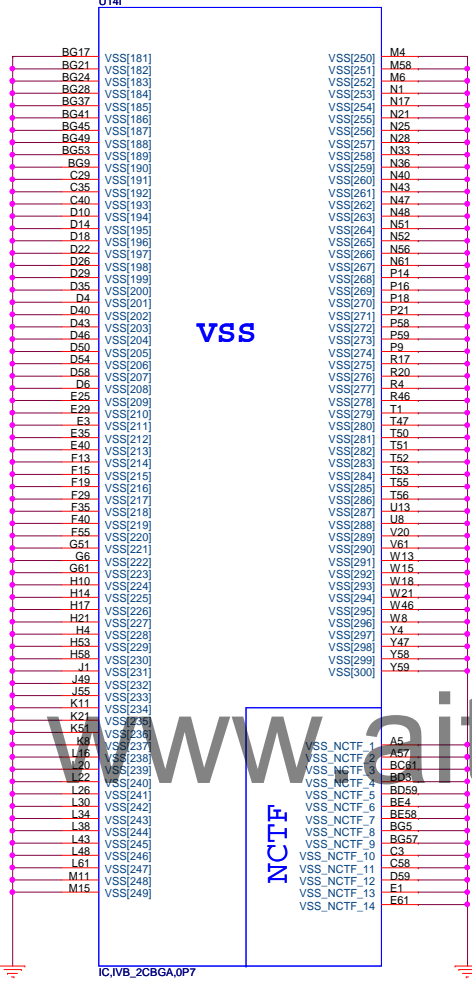
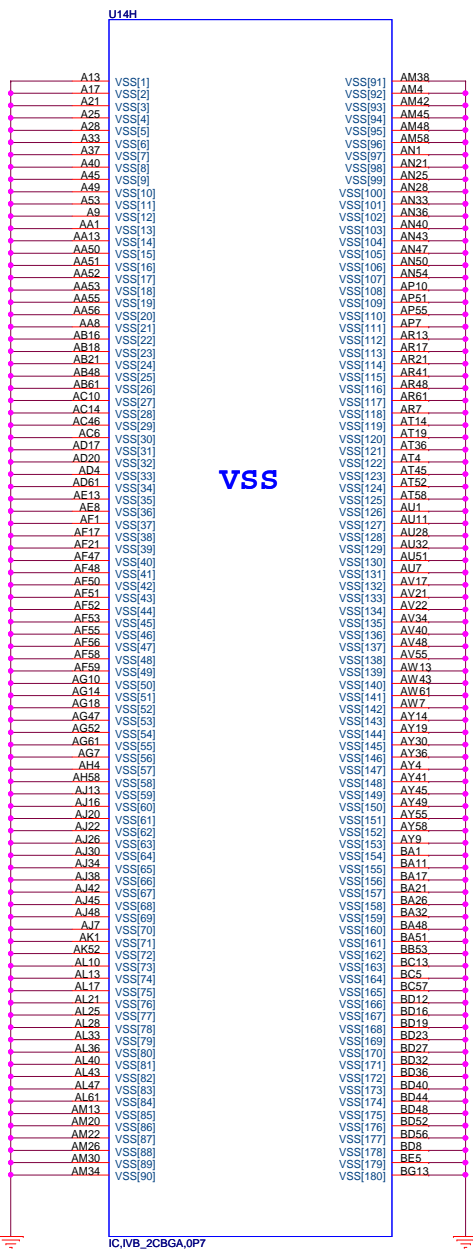




Ivy Bridge Processor (DDR3)





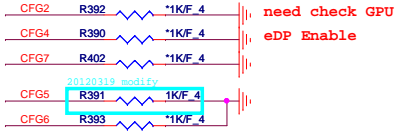


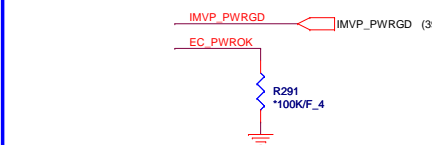
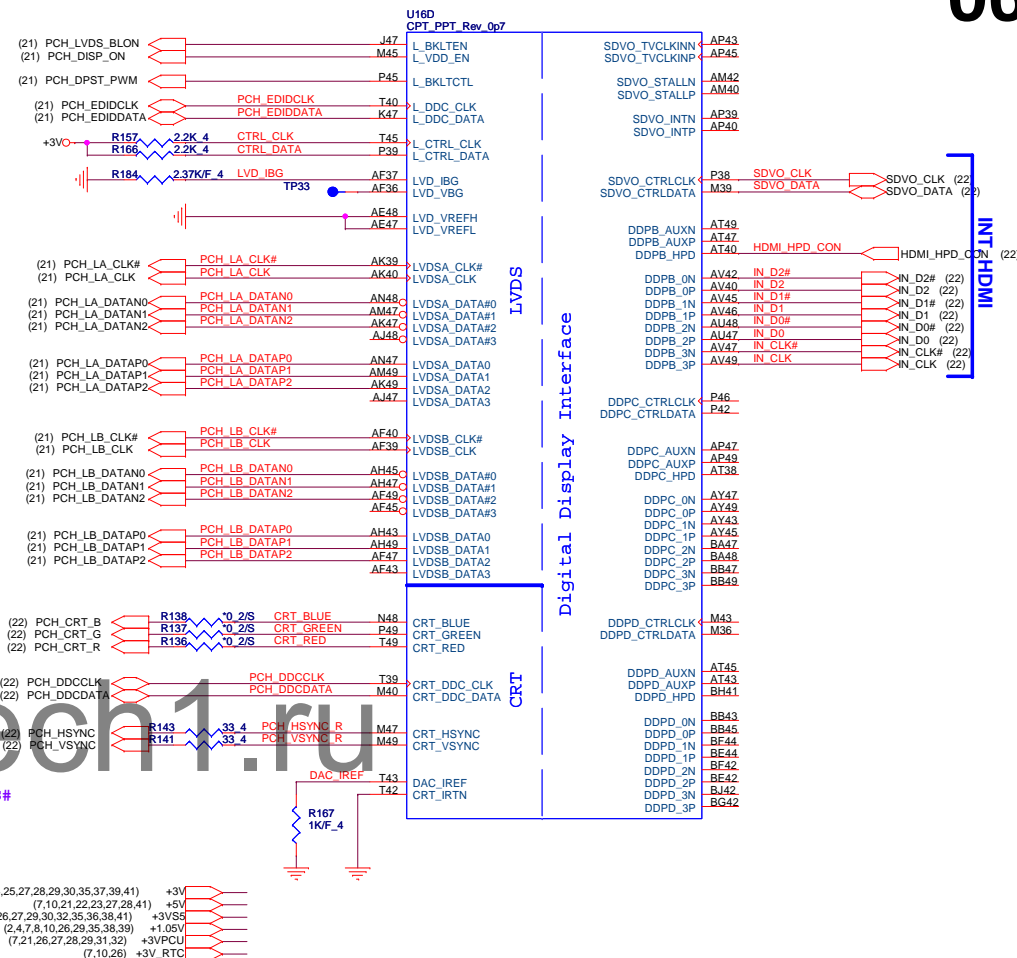
CFG[6:5] (PCIe Port Bifurcation Straps)
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

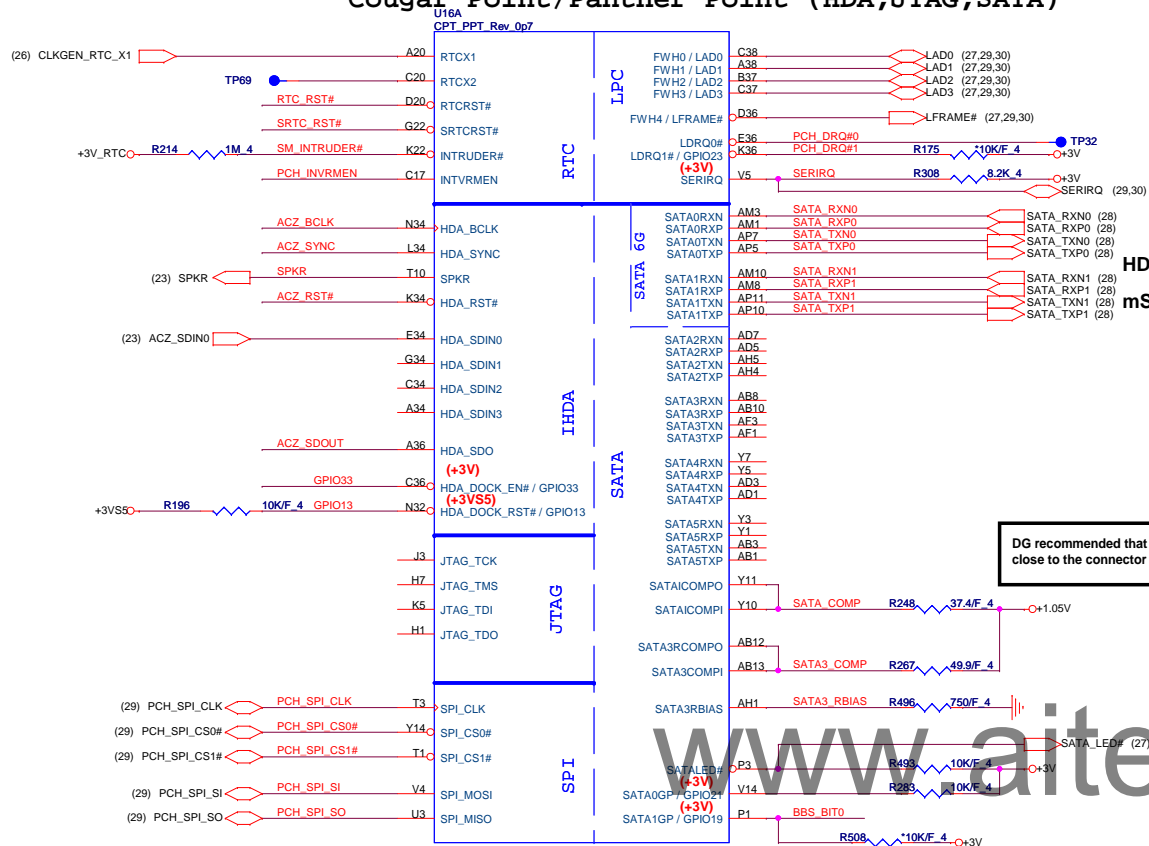
	1	0
CFG2 (PCIe Static x16 Lane Numbering Reversal.)	Normal Operation(Default)	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP





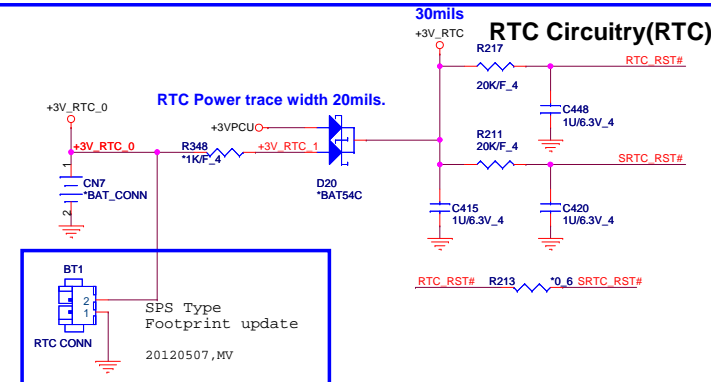
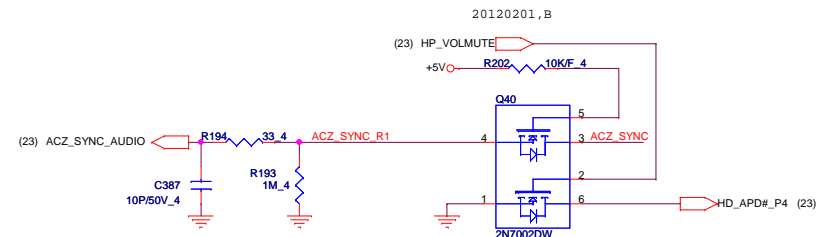
On Die DSW VR Enable
High = Enable (Default) Low = Disable

Cougar Point/Panther Point (HDA,JTAG,SATA)

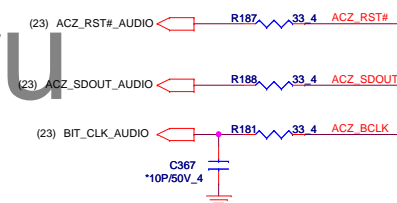


HDD0 (SATA3 6.0Gb/s)
mSATA (SATA3 6Gb/s)

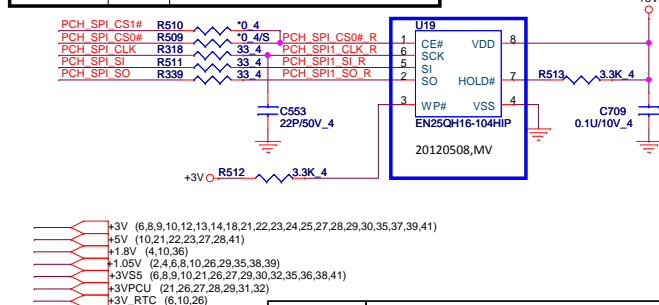
DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.



HDA Bus(CLG)



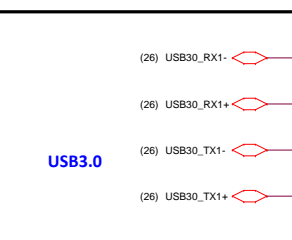
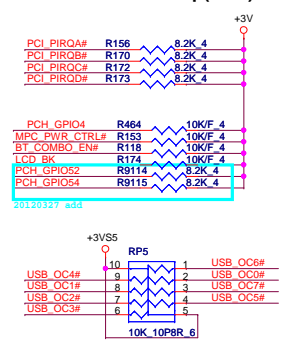
Vender	Size	P/N
EON	2MB	AKE38ZN0Q00 (EN25QH16-104HIP)
AMIC	2MB	AKE38ZN0802 (A25LQ16M-F/Q)
Socket		DG008000031



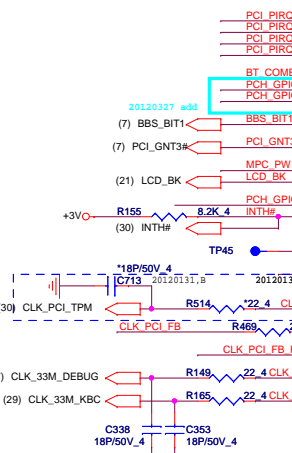
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V _{CC} R286 *1K/F 4 SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V _{CC} R121 *1K/F 4 PCI_GNT3# (8)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V _{RTC0} R223 330K 4 PCH_INVRMEN
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R177 *1K/F 4 ACZ_SDOUT (29)
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK		
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V _{CC} R262 *1K/F 4 INV_ALE (8)
DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm	+1.8V _{CC} R479 2.2K 4 R477 1K/F 4 DF_TVS (9) H_SNB_IVB# (2)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V _{SS0} R186 1K/F 4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	Rising edge of PWROK	1 = Override 0 = Default (weak pull-down 20K)	+3V _{SS0} R182 *1K/F 4 ACZ_SDOUT

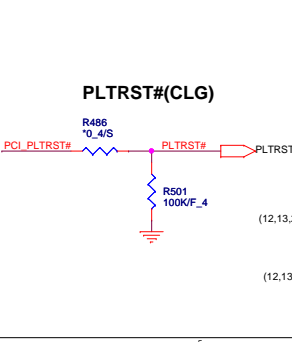
PCI/USBOC# Pull-up(CLG)



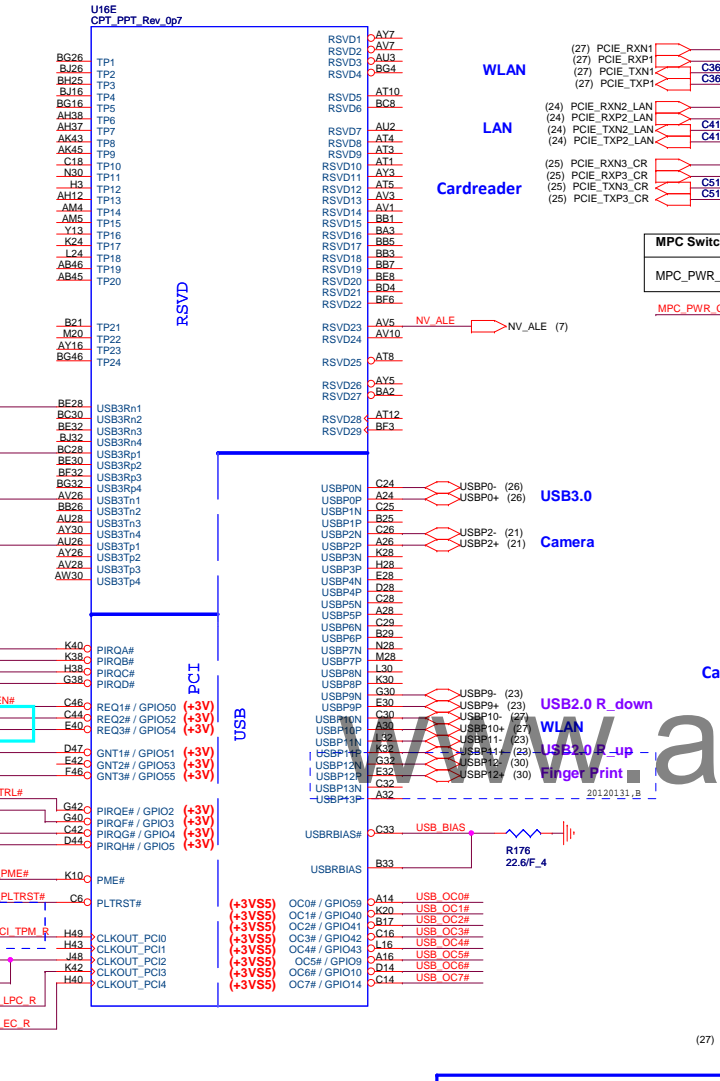
20111130 Modify USB3.0 for HM70



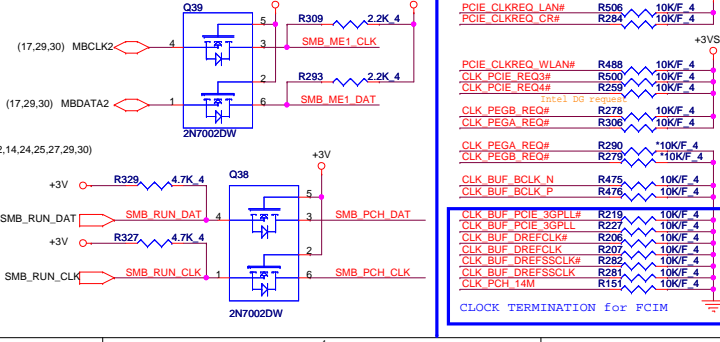
PLTRST#(CLG)



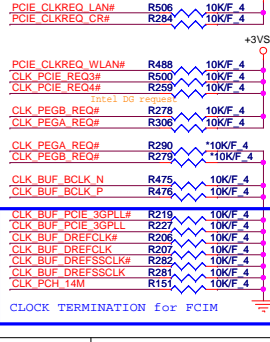
Cougar Point-M/Panther Point (PCI,USB,NVRAM)



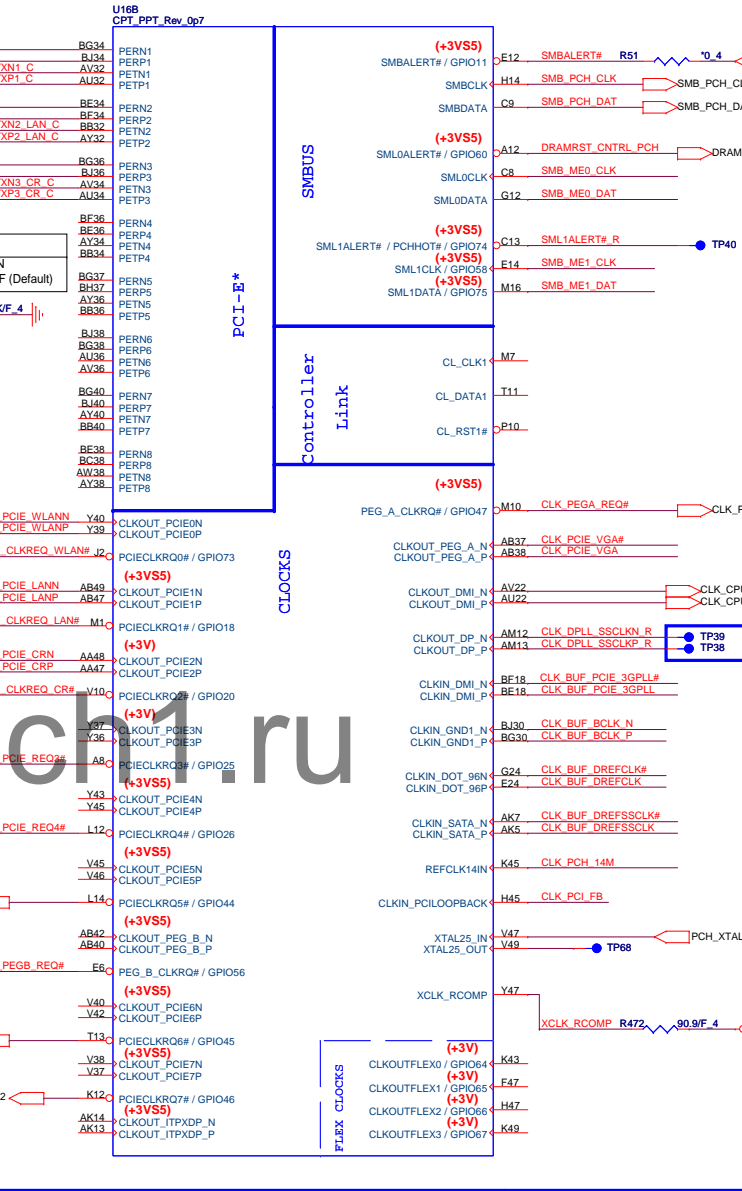
SMBus/Pull-up(CLG)



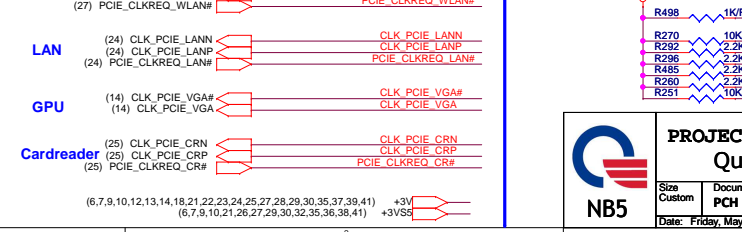
CLK REQ/Strap Pin(CLG)



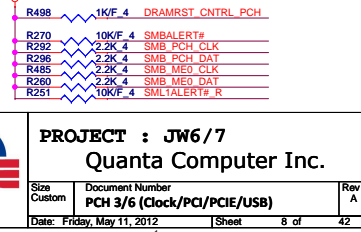
Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



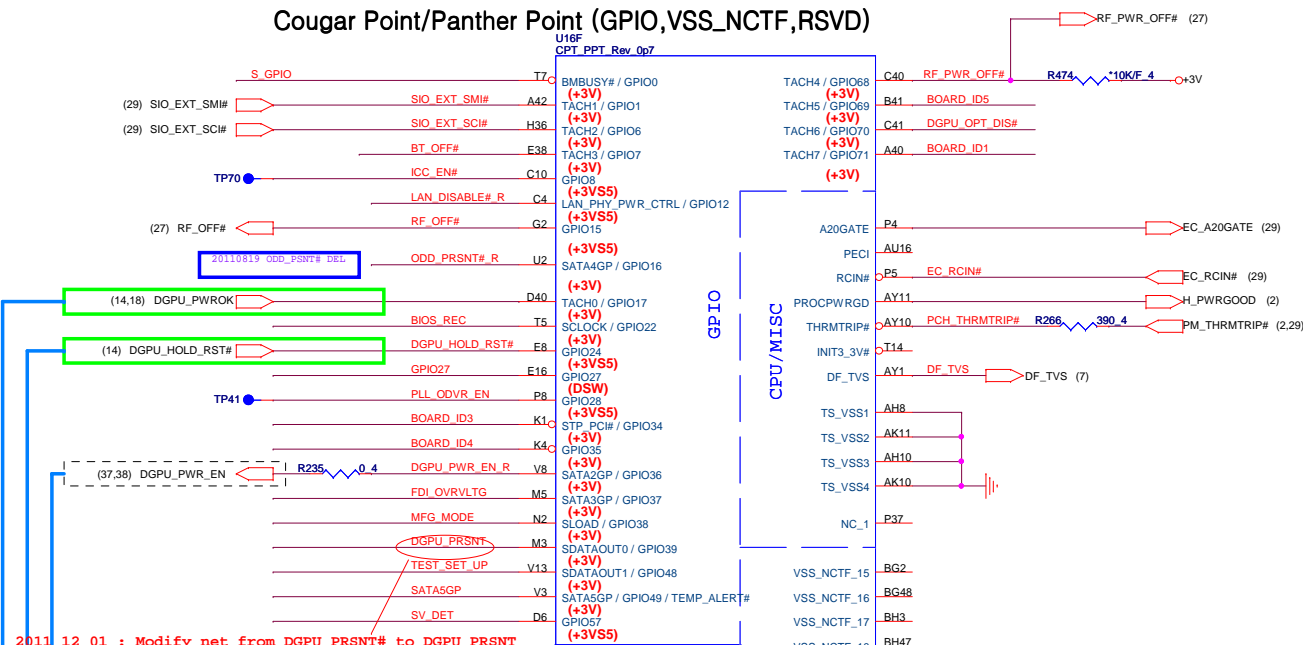
PCI Clock



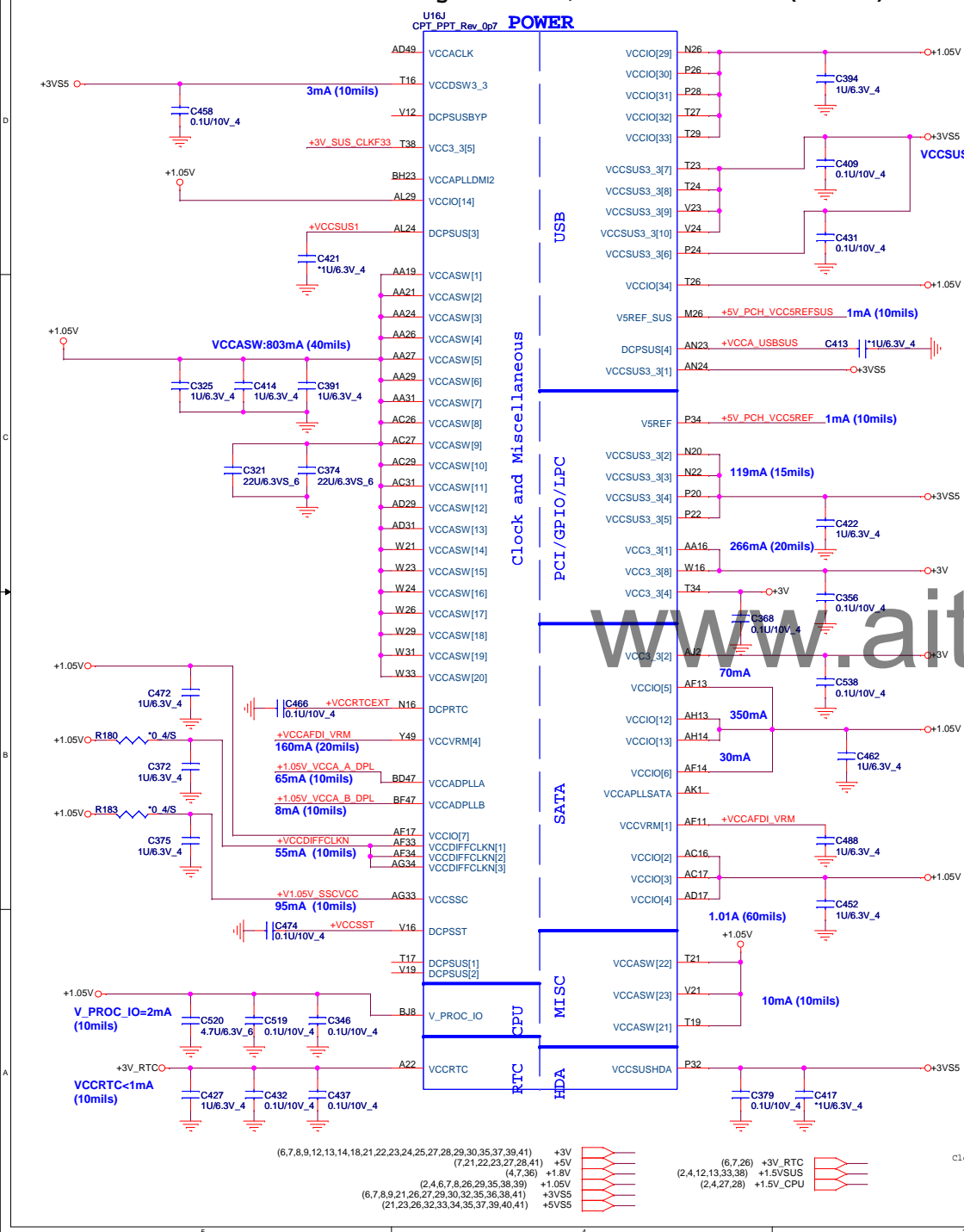
SMBus/Pull-up(CLG)



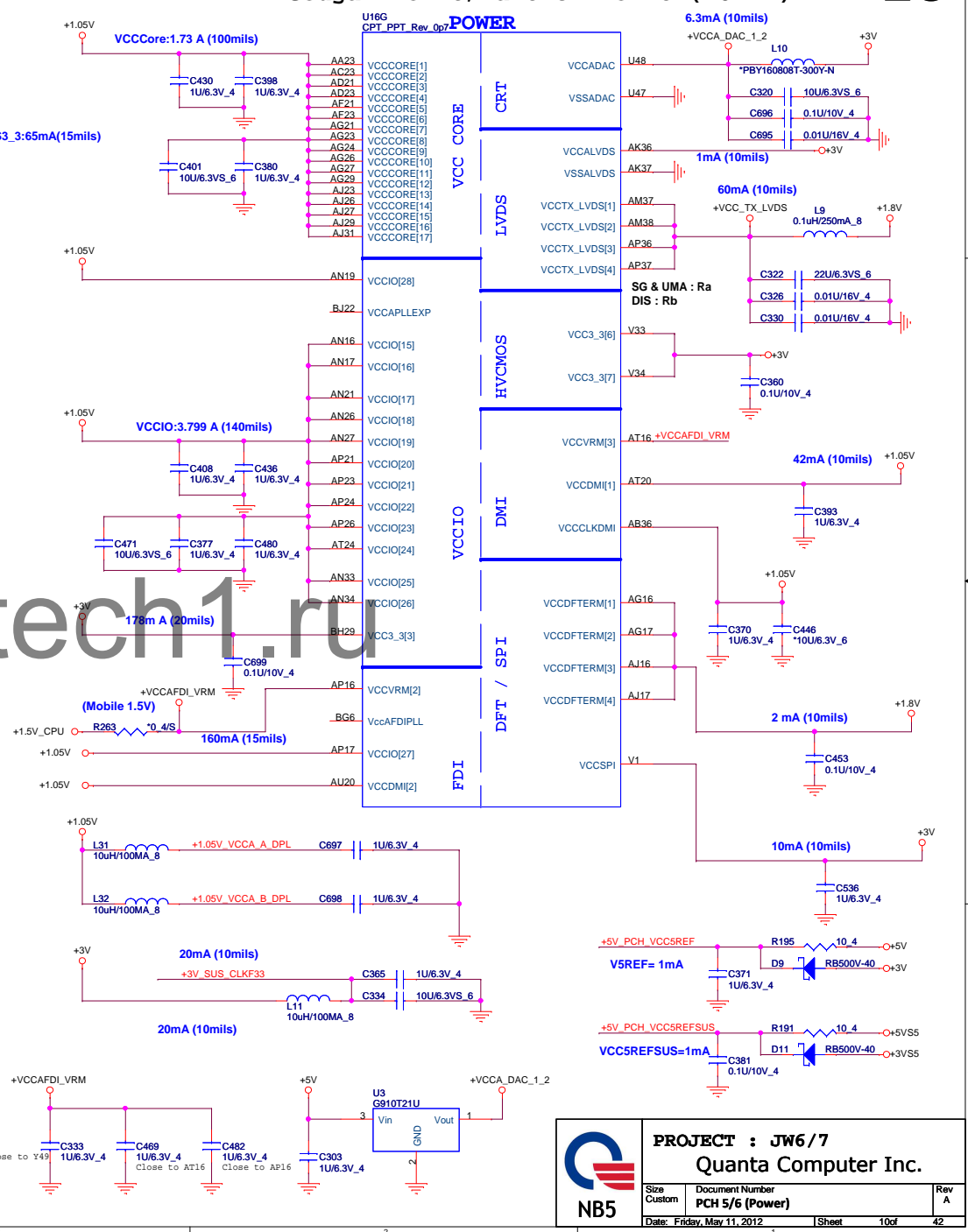
Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



Cougar Point/Panther Point (POWER)



Cougar Point/Panther Point (POWER)



Cougar Point/Panther Point (GND)

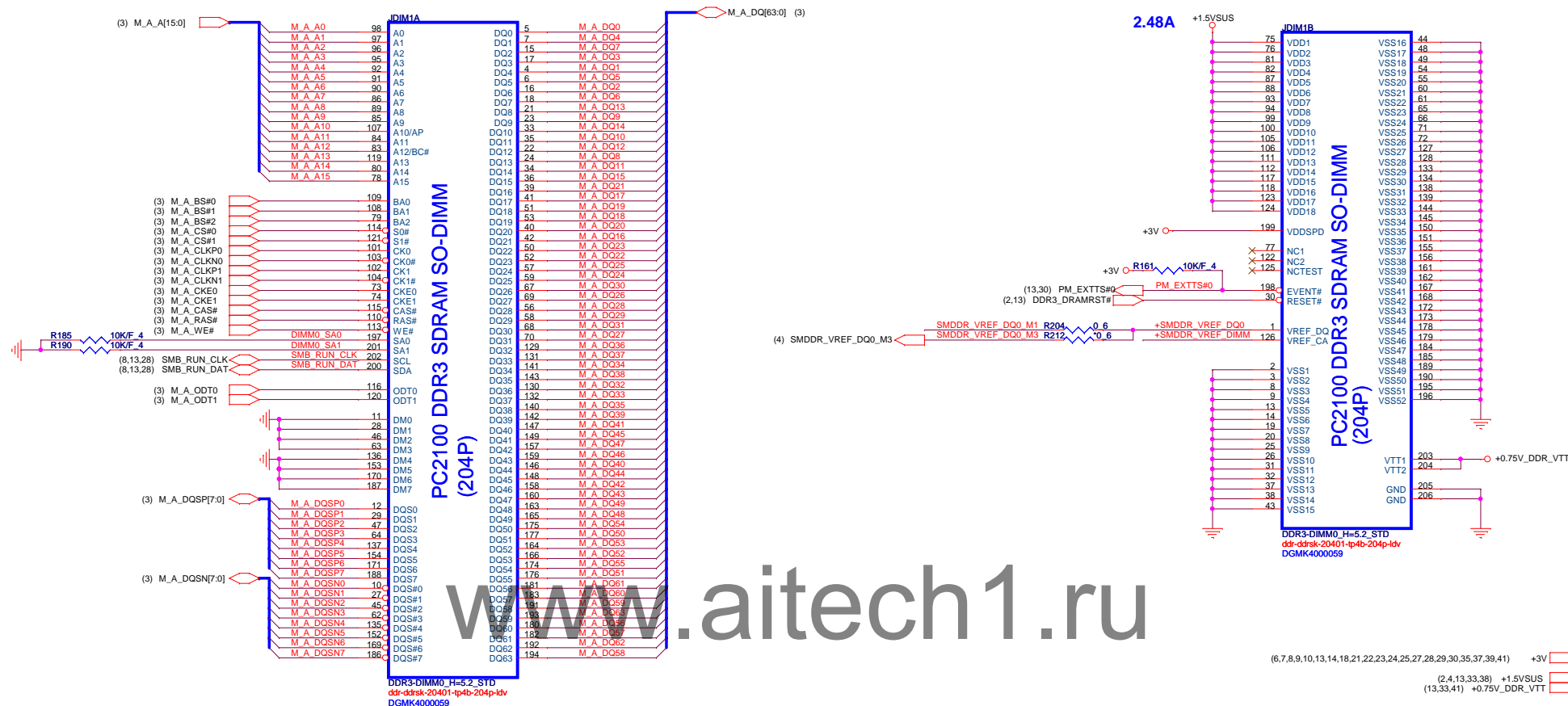
U16I
CPT PPT Rev Op7

AY4	VSS[159]	VSS[259]	H46
AY42	VSS[160]	VSS[260]	K18
AY46	VSS[161]	VSS[261]	K26
AY8	VSS[162]	VSS[262]	K39
B11	VSS[163]	VSS[263]	K46
B19	VSS[164]	VSS[264]	K7
B23	VSS[165]	VSS[265]	L18
B27	VSS[166]	VSS[266]	L2
B31	VSS[167]	VSS[267]	L20
B35	VSS[168]	VSS[268]	L26
B39	VSS[169]	VSS[269]	L28
B7	VSS[170]	VSS[270]	L36
F45	VSS[171]	VSS[271]	L48
BB12	VSS[172]	VSS[272]	M12
BB16	VSS[173]	VSS[273]	M18
BB20	VSS[174]	VSS[274]	M22
BB22	VSS[175]	VSS[275]	M24
BB24	VSS[176]	VSS[276]	M30
BB28	VSS[177]	VSS[277]	M32
BB30	VSS[178]	VSS[278]	M34
BB38	VSS[179]	VSS[279]	M38
BB4	VSS[180]	VSS[280]	M4
BB46	VSS[181]	VSS[281]	M42
BC14	VSS[182]	VSS[282]	M46
BC18	VSS[183]	VSS[283]	M8
BC2	VSS[184]	VSS[284]	N18
BC22	VSS[185]	VSS[285]	P30
BC26	VSS[186]	VSS[286]	P47
BC32	VSS[187]	VSS[287]	P7
BC34	VSS[188]	VSS[288]	R48
BC36	VSS[189]	VSS[289]	T12
BC40	VSS[190]	VSS[290]	T31
BC42	VSS[191]	VSS[291]	T4
BC48	VSS[192]	VSS[292]	W34
BD46	VSS[193]	VSS[293]	T46
BD5	VSS[194]	VSS[294]	T47
BE22	VSS[195]	VSS[295]	T8
BE26	VSS[196]	VSS[296]	V11
BE40	VSS[197]	VSS[297]	V17
BE10	VSS[198]	VSS[298]	V26
BE12	VSS[199]	VSS[299]	V27
BE16	VSS[200]	VSS[300]	V29
BF20	VSS[201]	VSS[301]	V31
BF22	VSS[202]	VSS[302]	V36
BF24	VSS[203]	VSS[303]	V38
BF26	VSS[204]	VSS[304]	V48
BF28	VSS[205]	VSS[305]	W17
BD3	VSS[206]	VSS[306]	W19
BF40	VSS[207]	VSS[307]	W2
BF38	VSS[208]	VSS[308]	W27
BF40	VSS[209]	VSS[309]	W48
BF8	VSS[210]	VSS[310]	Y12
BG17	VSS[211]	VSS[311]	Y38
BG21	VSS[212]	VSS[312]	Y42
BG33	VSS[213]	VSS[313]	Y46
BG33	VSS[214]	VSS[314]	Y8
BG44	VSS[215]	VSS[315]	Y8
BG8	VSS[216]	VSS[316]	Y8
BH11	VSS[217]	VSS[317]	Y8
BH15	VSS[218]	VSS[318]	Y8
BH17	VSS[219]	VSS[319]	Y8
BH19	VSS[220]	VSS[320]	Y8
H10	VSS[221]	VSS[321]	Y8
BH27	VSS[222]	VSS[322]	Y8
BH31	VSS[223]	VSS[323]	Y8
BH33	VSS[224]	VSS[324]	Y8
BH35	VSS[225]	VSS[325]	Y8
BH39	VSS[226]	VSS[326]	Y8
BH43	VSS[227]	VSS[327]	Y8
BH7	VSS[228]	VSS[328]	Y8
D3	VSS[229]	VSS[329]	Y8
D12	VSS[230]	VSS[330]	Y8
D16	VSS[231]	VSS[331]	Y8
D18	VSS[232]	VSS[332]	Y8
D22	VSS[233]	VSS[333]	Y8
D24	VSS[234]	VSS[334]	Y8
D26	VSS[235]	VSS[335]	Y8
D30	VSS[236]	VSS[336]	Y8
D32	VSS[237]	VSS[337]	Y8
D34	VSS[238]	VSS[338]	Y8
D38	VSS[239]	VSS[339]	Y8
D42	VSS[240]	VSS[340]	Y8
D8	VSS[241]	VSS[341]	Y8
E18	VSS[242]	VSS[342]	Y8
E26	VSS[243]	VSS[343]	Y8
G18	VSS[244]	VSS[344]	Y8
G20	VSS[245]	VSS[345]	Y8
G26	VSS[246]	VSS[346]	Y8
G28	VSS[247]	VSS[347]	Y8
G36	VSS[248]	VSS[348]	Y8
G48	VSS[249]	VSS[349]	Y8
H12	VSS[250]	VSS[350]	Y8
H18	VSS[251]	VSS[351]	Y8
H22	VSS[252]	VSS[352]	Y8
H24	VSS[253]		
H26	VSS[254]		
H30	VSS[255]		
H32	VSS[256]		
H34	VSS[257]		
F3	VSS[258]		

Cougar Point/Panther Point (GND)

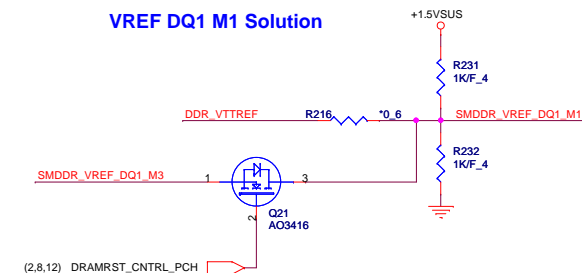
U16H
CPT PPT Rev Op7

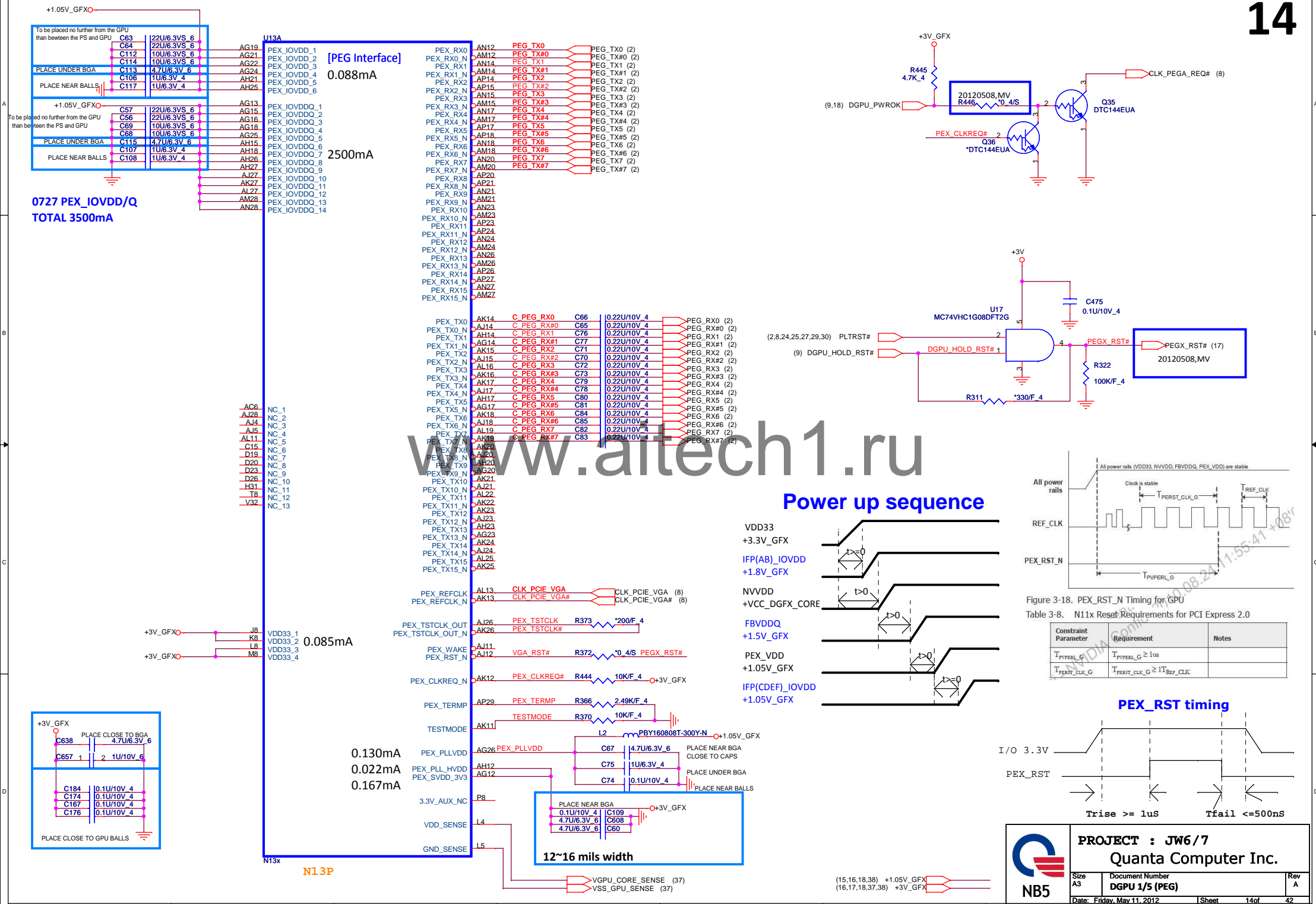
H5	VSS[0]	VSS[80]	AK38
AA17	VSS[1]	VSS[81]	AK4
AA2	VSS[2]	VSS[82]	AK42
AA3	VSS[3]	VSS[83]	AK46
AA33	VSS[4]	VSS[84]	AK8
AA34	VSS[5]	VSS[85]	AL16
AB11	VSS[6]	VSS[86]	AL17
AB14	VSS[7]	VSS[87]	AL19
AB39	VSS[8]	VSS[88]	AL2
AB4	VSS[9]	VSS[89]	AL21
AB43	VSS[10]	VSS[90]	AL23
AB5	VSS[11]	VSS[91]	AL26
AB7	VSS[12]	VSS[92]	AL27
AC19	VSS[13]	VSS[93]	AL31
AC2	VSS[14]	VSS[94]	AL33
AC21	VSS[15]	VSS[95]	AL34
AC24	VSS[16]	VSS[96]	AL48
AC33	VSS[17]	VSS[97]	AM11
AC34	VSS[18]	VSS[98]	AM14
AC48	VSS[19]	VSS[99]	AM36
AD10	VSS[20]	VSS[100]	AM39
AD11	VSS[21]	VSS[101]	AM43
AD12	VSS[22]	VSS[102]	AM45
AD13	VSS[23]	VSS[103]	AM46
AD19	VSS[24]	VSS[104]	AM7
AD24	VSS[25]	VSS[105]	AN2
AD26	VSS[26]	VSS[106]	AN29
AD27	VSS[27]	VSS[107]	AN31
AD33	VSS[28]	VSS[108]	AP12
AD34	VSS[29]	VSS[109]	AP19
AD36	VSS[30]	VSS[110]	AP28
AD37	VSS[31]	VSS[111]	AP30
AD38	VSS[32]	VSS[112]	AP32
AD39	VSS[33]	VSS[113]	AP38
AD40	VSS[34]	VSS[114]	AP4
AD42	VSS[35]	VSS[115]	AP42
AD43	VSS[36]	VSS[116]	AP46
AD45	VSS[37]	VSS[117]	AP8
AD46	VSS[38]	VSS[118]	AR2
AD8	VSS[39]	VSS[119]	AR48
AE2	VSS[40]	VSS[120]	AT11
AE3	VSS[41]	VSS[121]	AT13
AE10	VSS[42]	VSS[122]	AT18
AF12	VSS[43]	VSS[123]	AT22
AD14	VSS[44]	VSS[124]	AT26
AD16	VSS[45]	VSS[125]	AT28
AF18	VSS[46]	VSS[126]	AT30
AF19	VSS[47]	VSS[127]	AT32
AF24	VSS[48]	VSS[128]	AT34
AF26	VSS[49]	VSS[129]	AT39
AF27	VSS[50]	VSS[130]	AT42
AF28	VSS[51]	VSS[131]	AT46
AF3	VSS[52]	VSS[132]	AT7
AF38	VSS[53]	VSS[133]	AU24
AF4	VSS[54]	VSS[134]	AU30
AF42	VSS[55]	VSS[135]	AV16
AF46	VSS[56]	VSS[136]	AV20
AF5	VSS[57]	VSS[137]	AV24
AF7	VSS[58]	VSS[138]	AV30
AF8	VSS[59]	VSS[139]	AV38
AG19	VSS[60]	VSS[140]	AV4
AG2	VSS[61]	VSS[141]	AV43
AG31	VSS[62]	VSS[142]	AV48
AG48	VSS[63]	VSS[143]	AW14
AH11	VSS[64]	VSS[144]	AW18
AH3	VSS[65]	VSS[145]	AW2
AH36	VSS[66]	VSS[146]	AW22
AH39	VSS[67]	VSS[147]	AW26
BE10	VSS[68]	VSS[148]	AW28
AH40	VSS[69]	VSS[149]	AW32
AH42	VSS[70]	VSS[150]	AW34
AH46	VSS[71]	VSS[151]	AW36
AH7	VSS[72]	VSS[152]	AW40
AJ19	VSS[73]	VSS[153]	AW48
AJ21	VSS[74]	VSS[154]	AV11
AJ24	VSS[75]	VSS[155]	AV12
AJ33	VSS[76]	VSS[156]	AY22
AJ34	VSS[77]	VSS[157]	AY28
AK12	VSS[78]	VSS[158]	
AK3	VSS[79]		

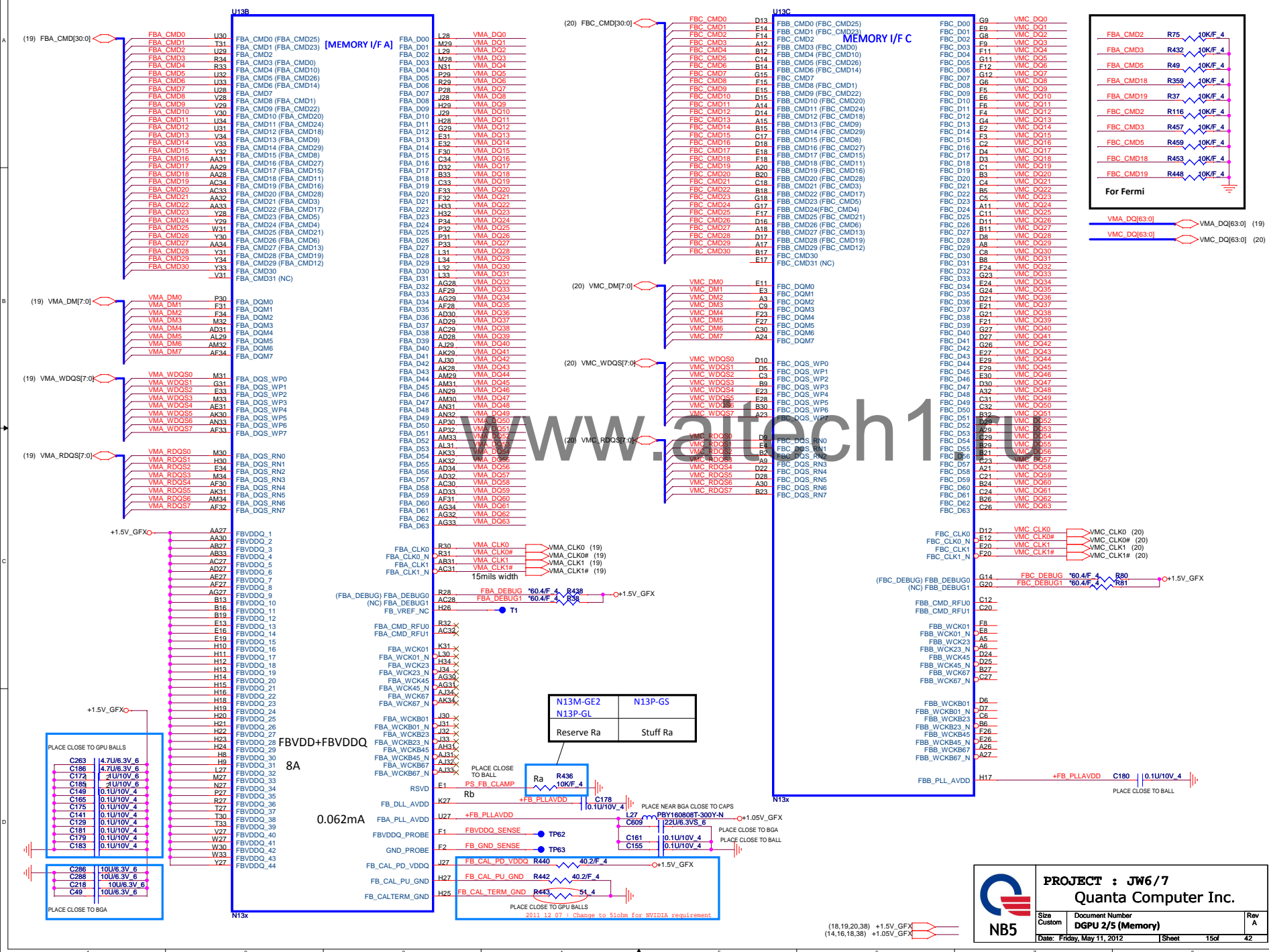




VREF DQ1 M1 Solution

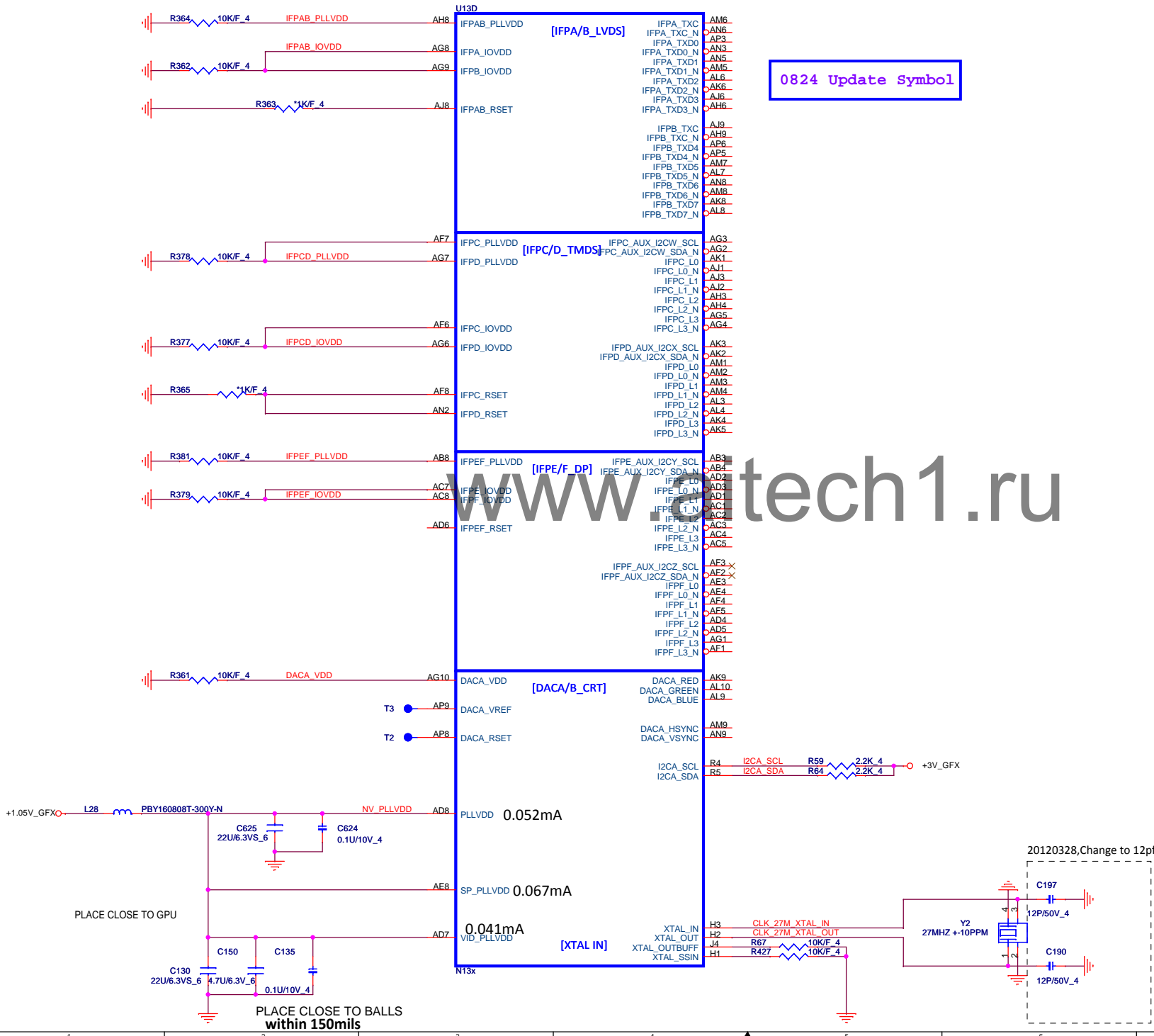






(14,15,18,38) +1.05V_GFX
(14,17,18,37,38) +3V_GFX

0824 Update Symbol



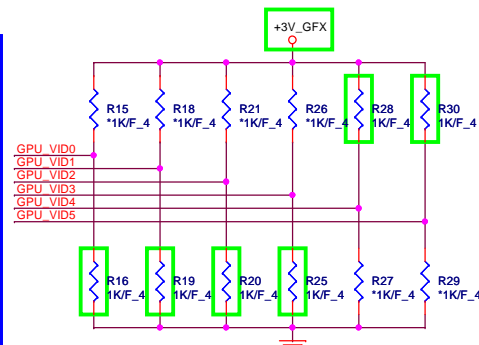
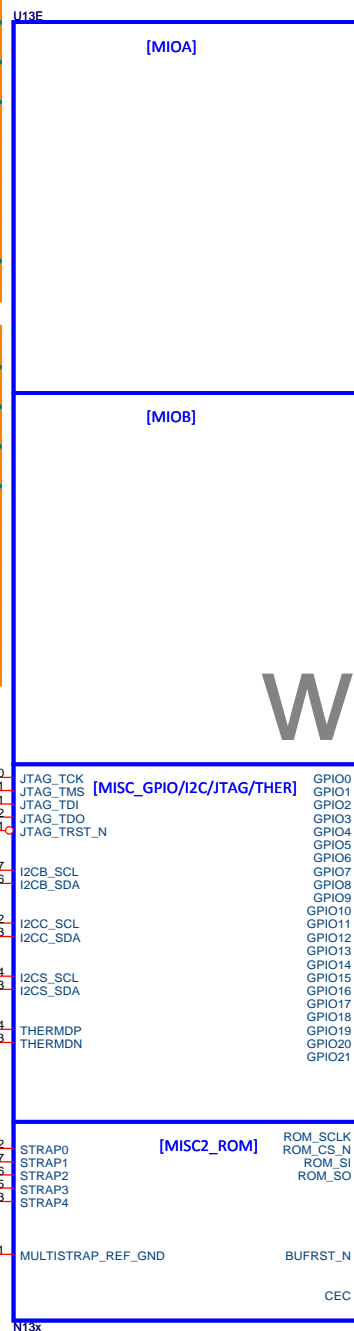
Net name	N13M-GE2	N13P-GS(QS)
ROM_SI		
ROM_SO	PD 10K	PU 10K
ROM_SCLK	PD 15K	PU 5K
STRAP0	PU 45K	PU 45K
STRAP1	PD 45K	PD 5K
STRAP2	PU 15K	PD 15K
STRAP3	UN-STUFF	PD 5K
STRAP4	UN-STUFF	PD 45K

Net name	N13P-GL
ROM_SI	
ROM_SO	PD 10K
ROM_SCLK	PD 15K
STRAP0	PU 45K
STRAP1	PD 5K
STRAP2	PU 10K
STRAP3	UN-STUFF
STRAP4	UN-STUFF

For N13M-GE2
ROM_SO PD 10K
ROM_SCLK PD 15K

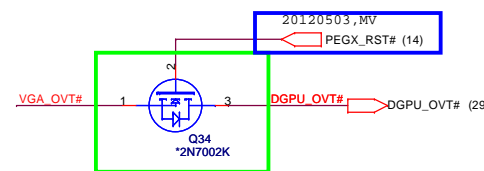
For N13P-GS
ROM_SO PU 10K
ROM_SCLK PU 5K

N13M-GE2-A1 ID:0X0DEA
N13P-GS ID:0X0FD2
N13P-GL-A1 ID:0X0DE9



VID 0 0 0 0 1 1 0 ---> 0.9V
VID 0 0 1 1 0 1 0 ---> 0.95V

N13P-GS-A2
N13P-GL-A1



Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Default: Hynix VRAM

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	1001
ROM_SCLK	PCI_DEVICE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0011
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVICE[3]	PCI_DEVICE[2]	PCI_DEVICE[1]	PCI_DEVICE[0]	0111
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	XXXX
STRAP4	RESERVED	PCI SPEED CHANGE GEN3	PCI_MAX SPEED	DP_PLL_VDD33	XXXX

For N13M-GE2, N13M-GS (QS)
Default: 2G Samsung

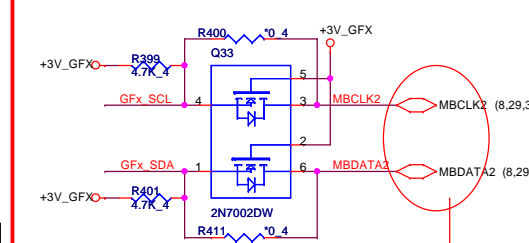
VRAM Configuration Table

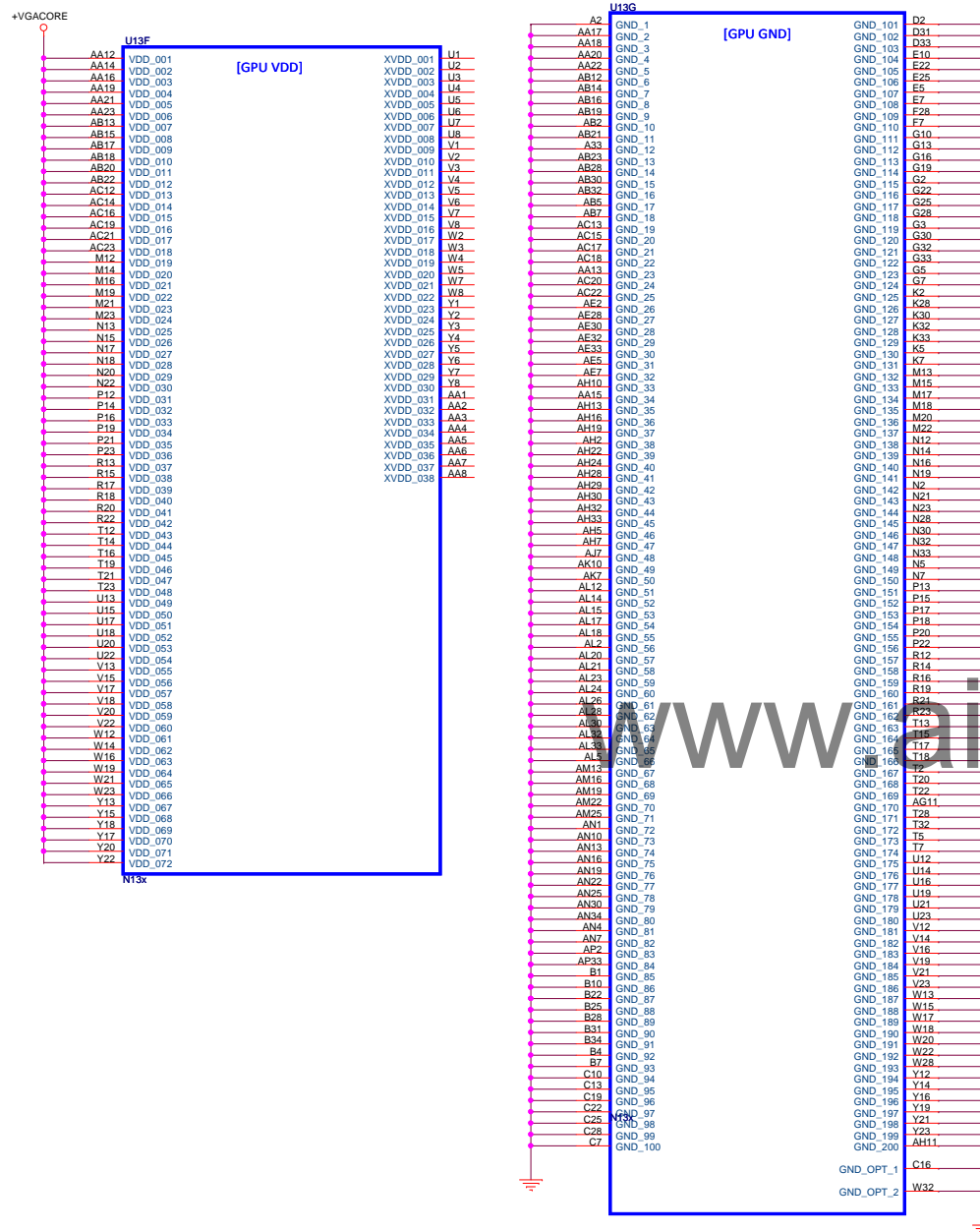
ROM_SI	
1G Hynix 64Mx16	-->15K PD
1G Samsung 64Mx16	-->20K PD
2G Hynix 128Mx16	-->35K PD
2G Samsung 128Mx16	-->45K PD

GPIO ASSIGNMENTS

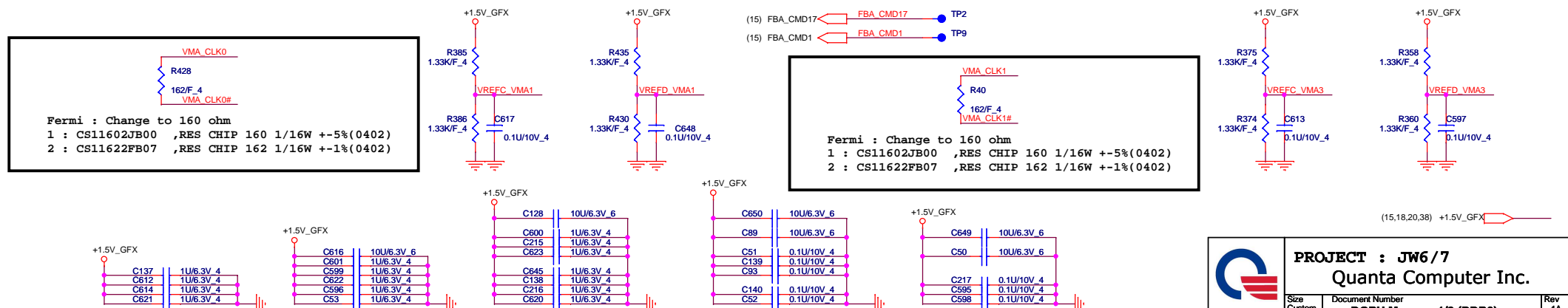
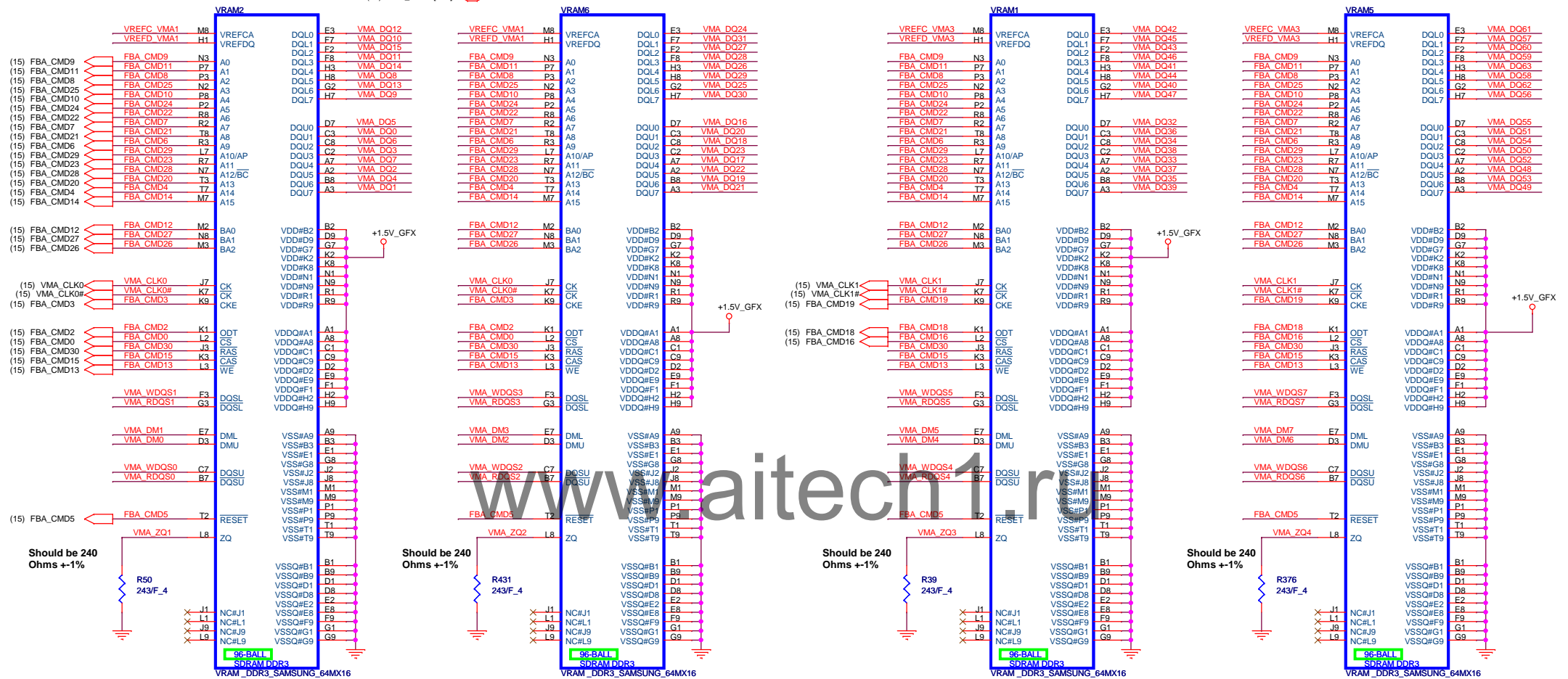
GPIO	I/O	PIN	USAGE
0	OUT	GPU_VID4	GPU CORE_VDD VID4
1	OUT	GPU_VID3	GPU CORE_VDD VID3
2	OUT	LCD_BL_PWM	LCD BACKLIGHT PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	GPU_VID1	GPU CORE_VDD VID1
6	OUT	GPU_VID2	GPU CORE_VDD VID2
7	OUT	3D VISION	3D VISION LEFT/RIGHT VISION
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF	MEMORY VREF CONTROL
11	OUT	GPU_VID0	GPU CORE_VDD VID0
12	IN	PWR_LEVEL	Power Detect ,HIGH=AC, LOW=DC
13	OUT	GPU_VID5	GPU CORE_VDD VID5
14	IN	HPD_AB	HOT PLUG DETECT FOR IFPAB
15	IN	HPD_C	HOT PLUG DETECT FOR IFPC
16	OUT	MEM VDD	MEMORY VDD CONTROL
17	IN	HPD_D	HOT PLUG DETECT FOR IFPD
18	IN	HPD_E	HOT PLUG DETECT FOR IFPE
19	IN	HPD_F	HOT PLUG DETECT FOR IFPF
20/21		RESERVE	

GFx SMBus Isolation



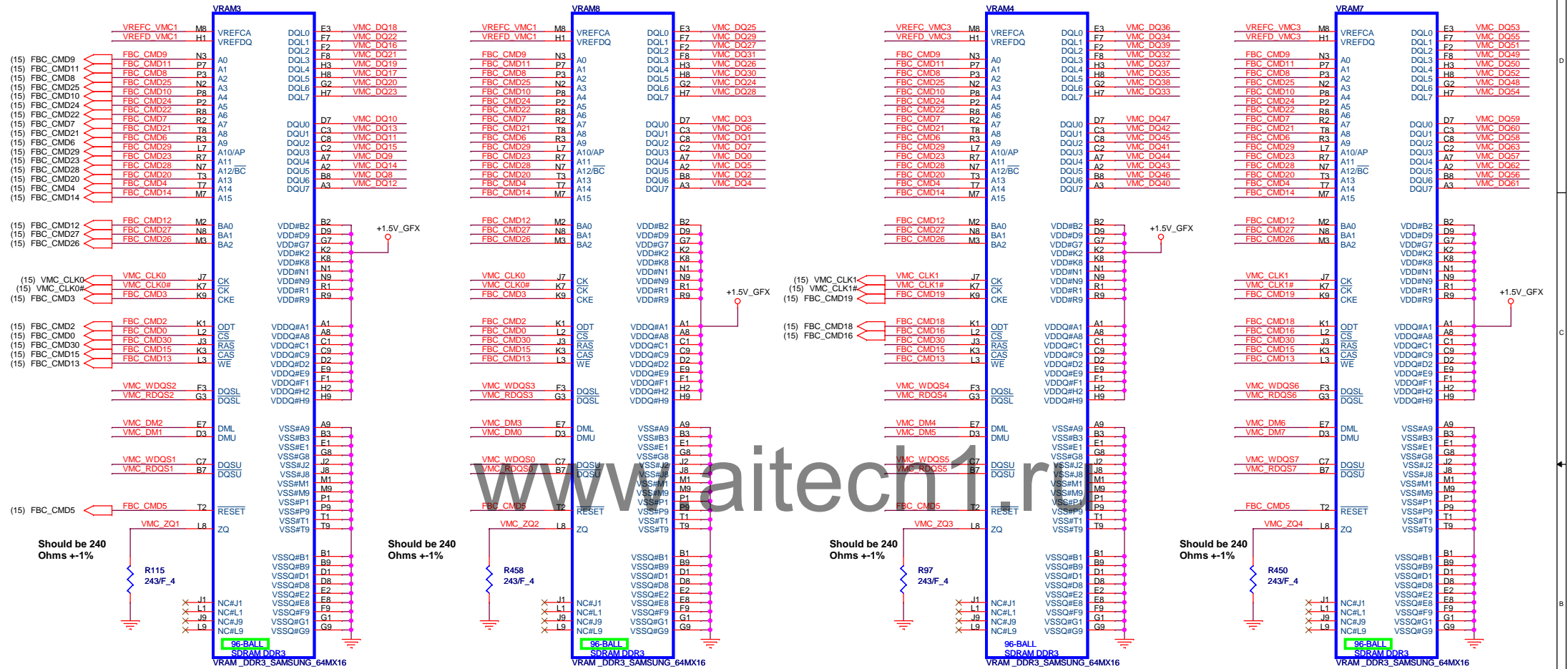


CHANNEL A: 256MB/512MB DDR3



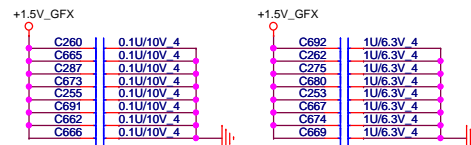
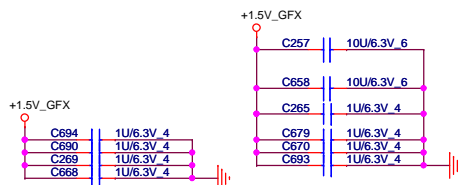
(15) VMC_DQ[63:0]
(15) VMC_DM[7:0]
(15) VMC_WDQS[7:0]
(15) VMC_RDQS[7:0]

CHANNEL B: 256MB/512MB DDR3



Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

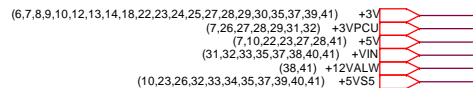
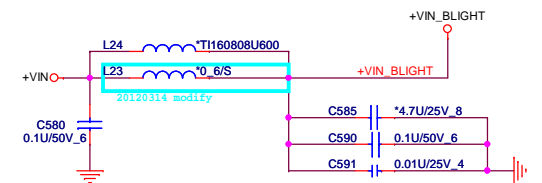
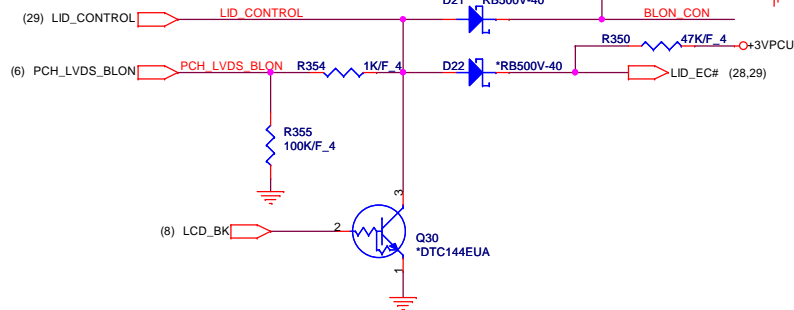
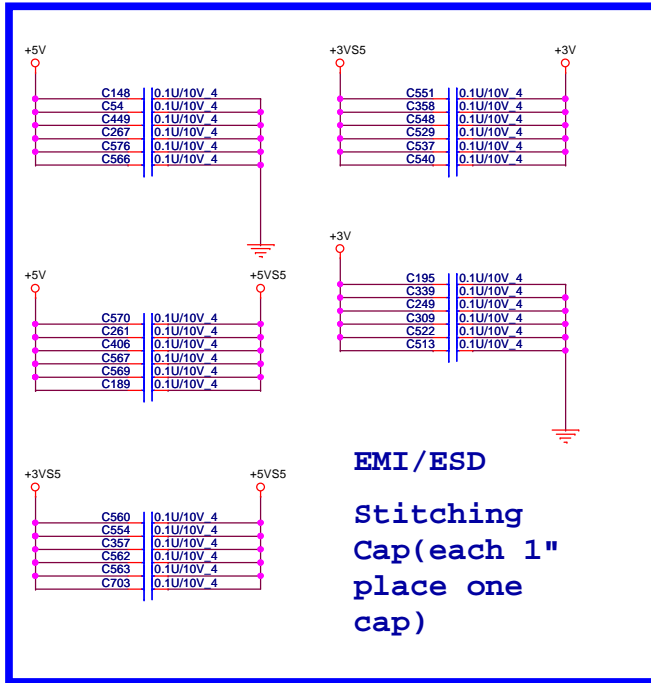
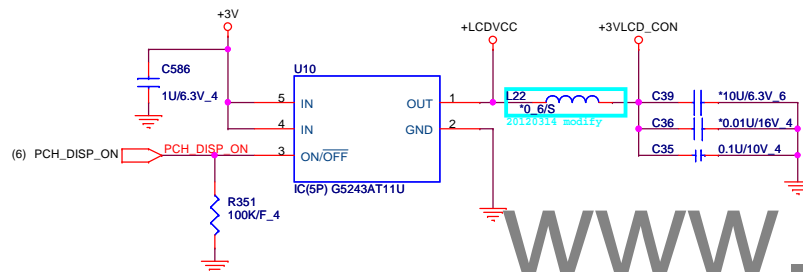
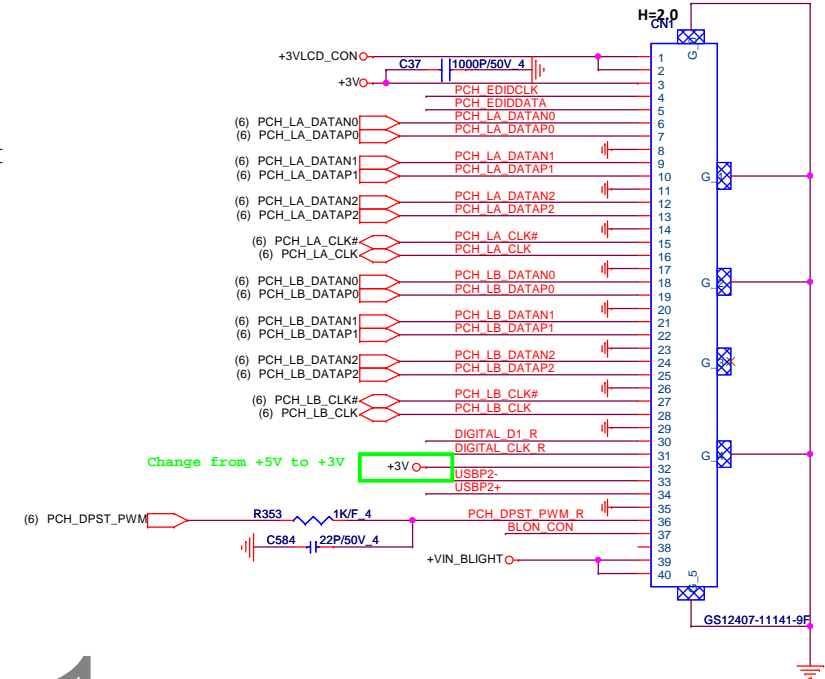
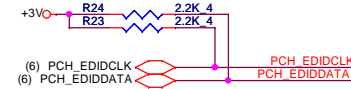
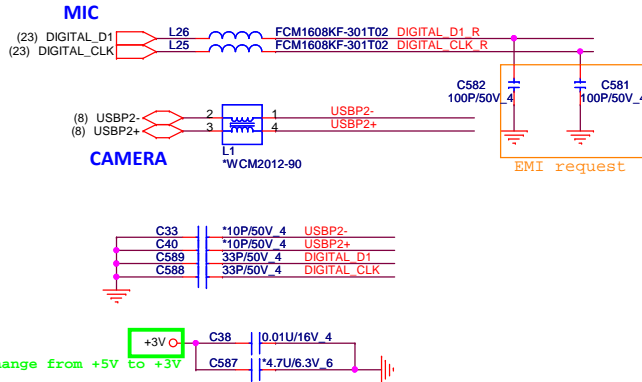
Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

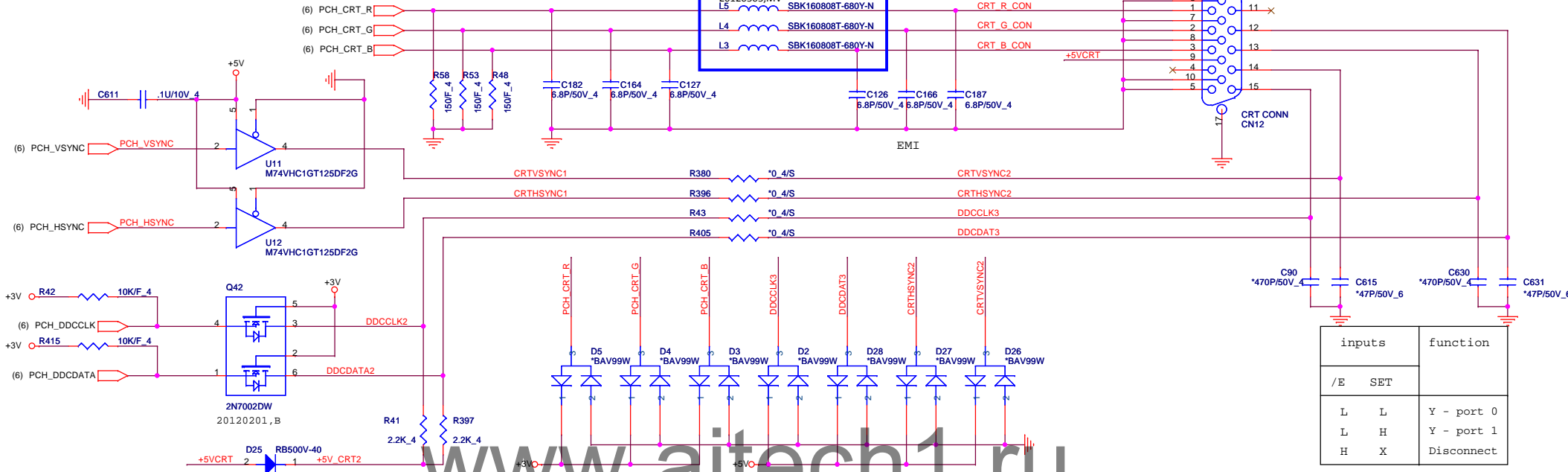
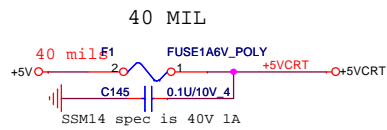


(15) FBC_CMD17 FBC_CMD17 TP26
(15) FBC_CMD1 FBC_CMD1 TP27

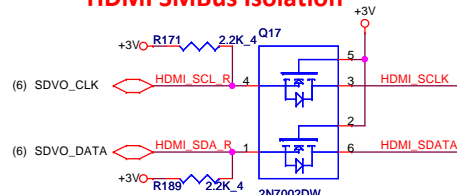
900MHz VRAM size:
Samsung 64Mx16, P/N = AKD5EGGT500
Samsung 128Mx16, P/N = AKD5MGWT500
Hynix 64Mx16, P/N = AKD5LZWTW02
Hynix 128Mx16, P/N = AKD5MGWTW00

USB Camera Connector



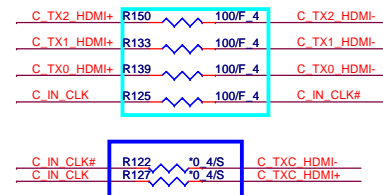


HDMI SMBus Isolation

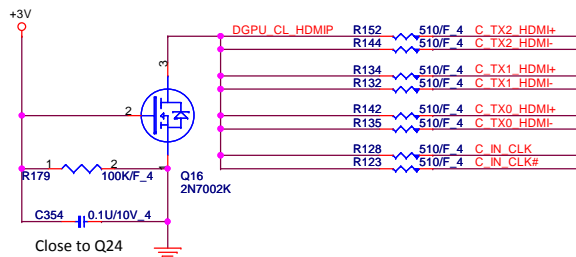
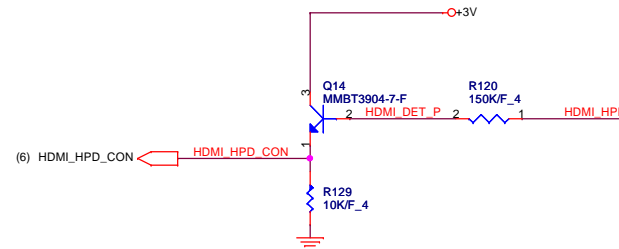
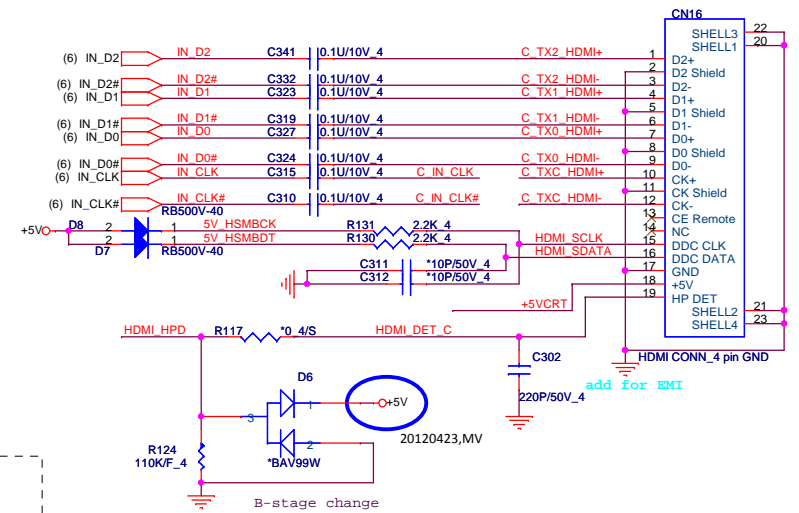


Close to HDMI connector

EMI Solution

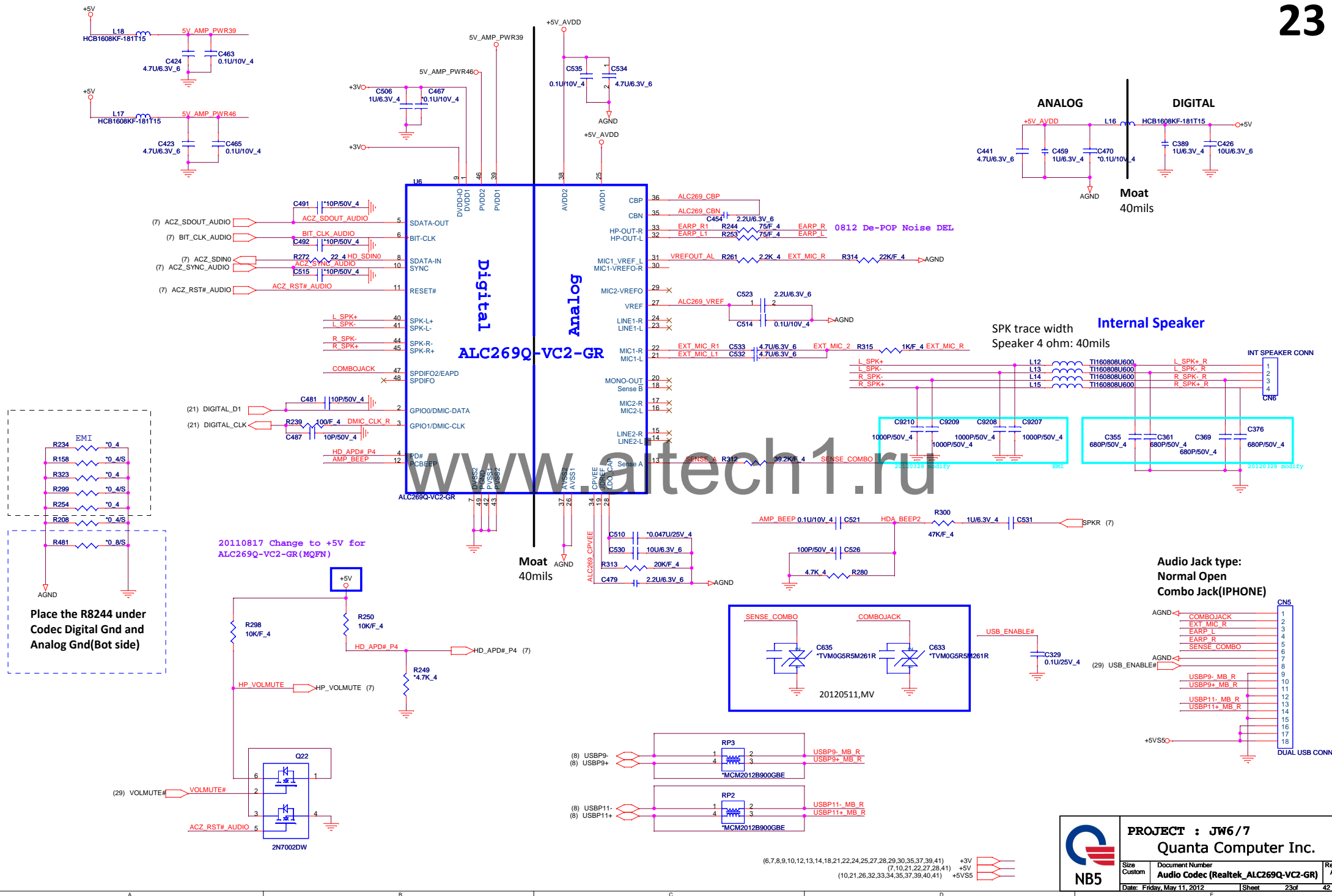


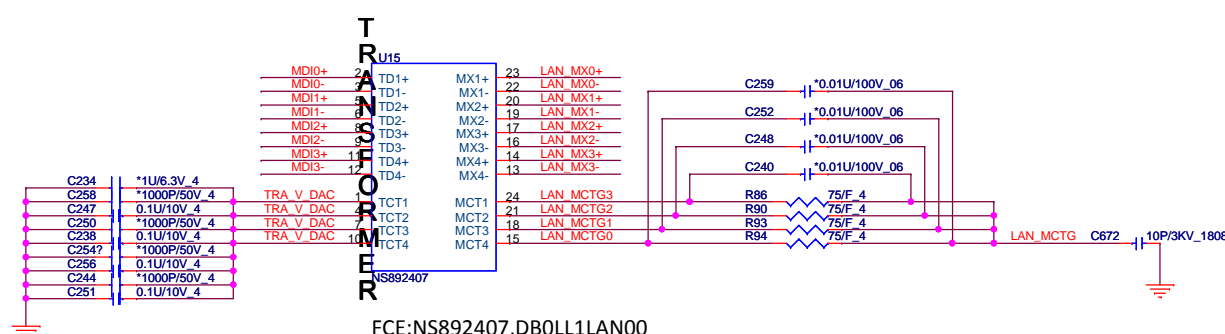
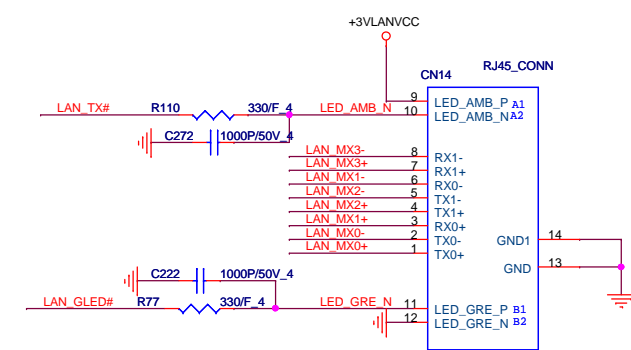
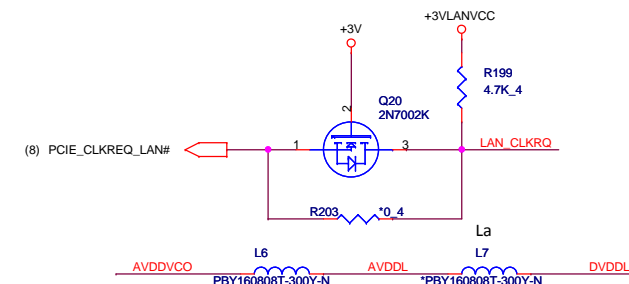
HDMI PORT



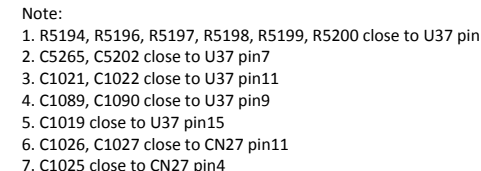
PROJECT : JW6/7
Quanta Computer Inc.

Size Custom Document Number CRT/HDMI Connector Rev A
Date: Friday, May 11, 2012 Sheet 22 of 42





FCE:NS892407,DB0LL1LAN00
BOT:GST5009B LF,DB0Z06LAN00

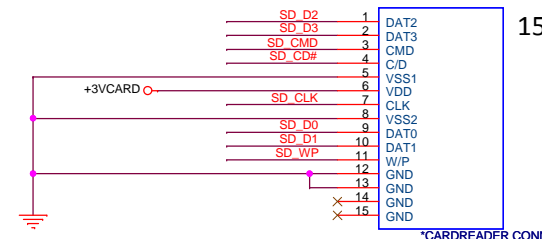


www.aitech1.ru

EMI Solution
Please help to close to connector

The diagram shows six signal lines, each connected to a capacitor and then to ground. The signal lines are labeled SD_CMD, SD_D0, SD_D1, SD_D2, SD_D3, and SD_CLK. The capacitors are labeled C503, C495, C494, C505, C504, and C496. Each capacitor is connected to ground and has a value of *5.6P/16V_4.

15" Only



H11

2

*O-JW6-2

H6

4

2

*INTEL-CPU-BKT3

H4

*H-C315I158D118P2

PAD1

1

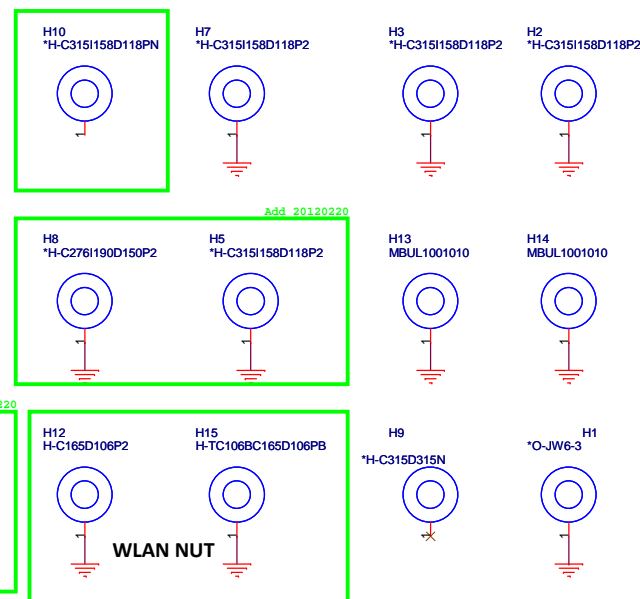
*SPAD-RE177X206NP

H16

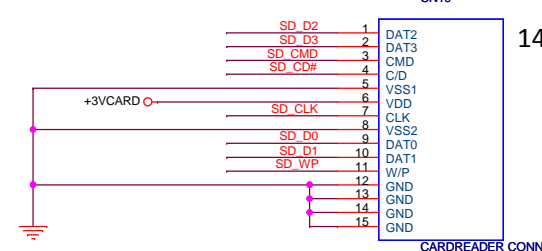
*H-C276I190D150P2

H17

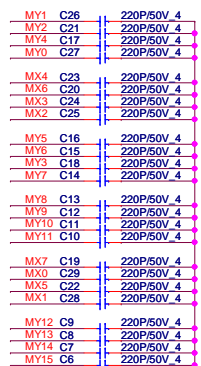
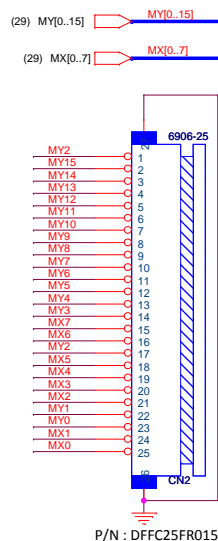
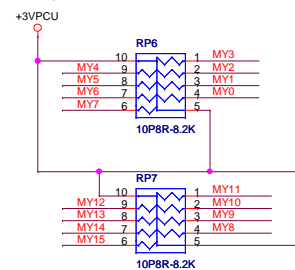
*H-C276I190D150P2



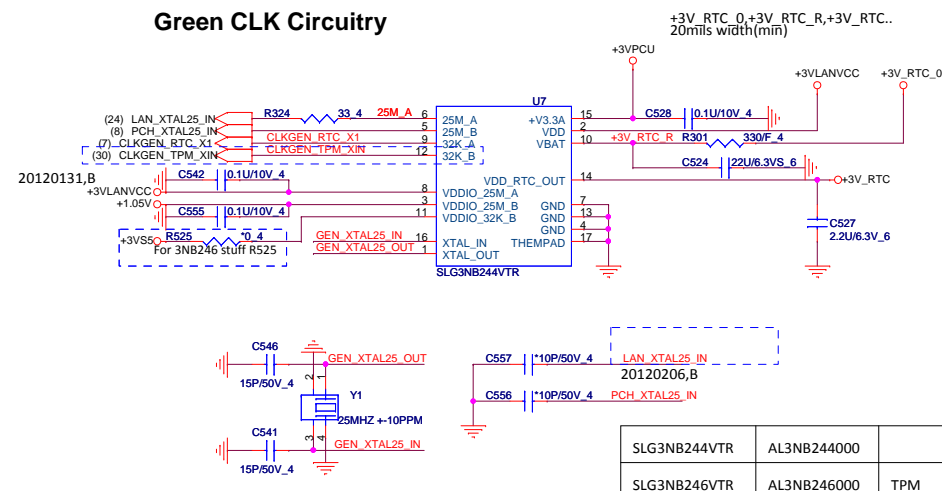
14" Only



Keyboard Connector



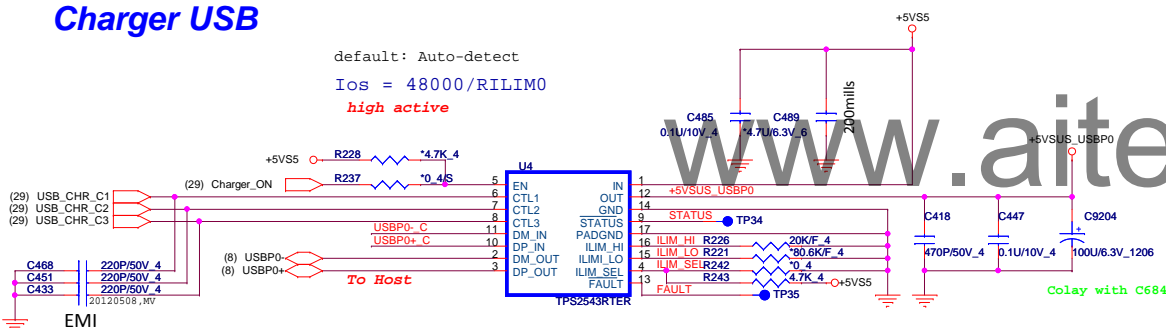
Green CLK Circuitry



SLG3NB244VTR	AL3NB244000	
SLG3NB246VTR	AL3NB246000	TPM

Charger USB

default: Auto-detect
 Ios = 48000/RILIMO
 high active



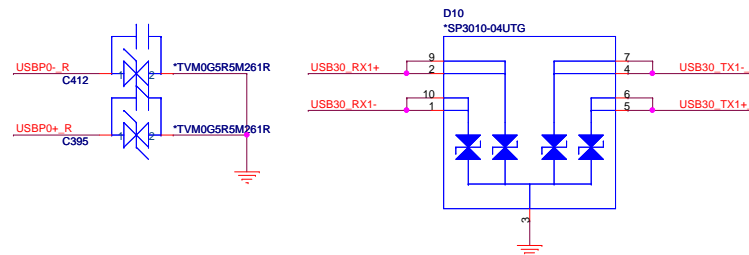
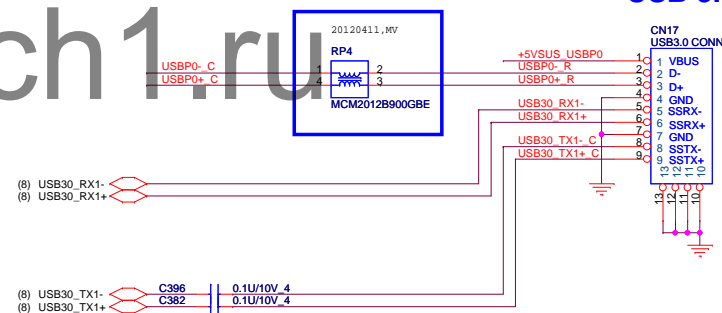
TPS2543/45 Control Truth Table

CTL1	CTL2	CTL3	ILIM_SEL	Charging Mode	Current Limit Setting	TPS2543 STATUS Output (active low)
0	0	0	1	Discharge	NA	off
0	0	1	1	DCP/auto	IOS_PW & ILIM_HI (1)	DCP load present
0	1	0	1	SDP	ILIM_HI	off
0	1	1	1	DCP/auto	ILIM_HI	DCP load present
1	1	0	1	SDP	ILIM_HI	off
1	1	1	1	CDP	ILIM_HI	CDP load present

(1) ILIM_HI: 20K(R5233), 2.4A

USB3.0 X 1/USB2.0 COMBO

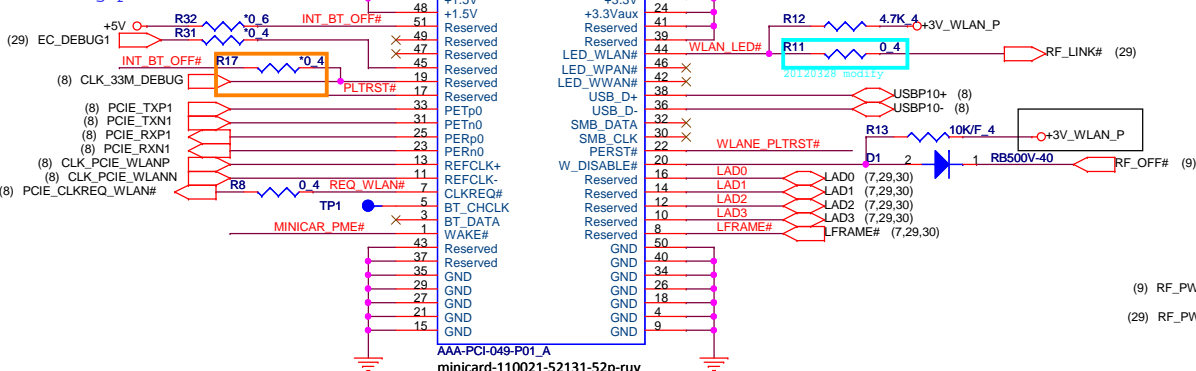
USB 3.0



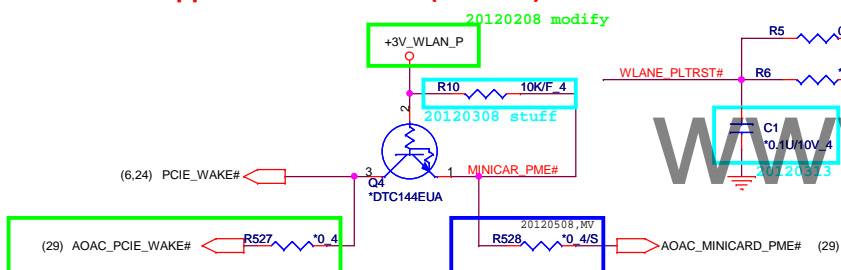
(10,21,23,32,33,34,35,37,39,40,41) +5VS5
 (7,21,27,28,29,31,32) +3VPCU

**Mini Card
WLAN/BT(Optional)**

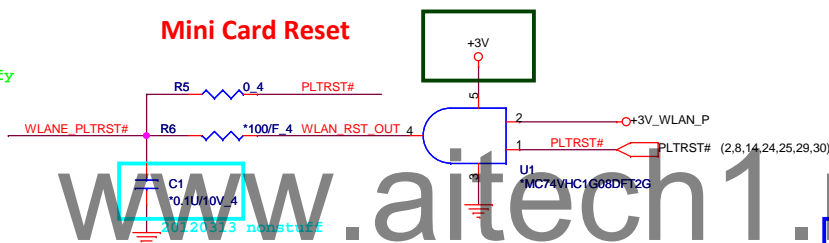
EC debug pin



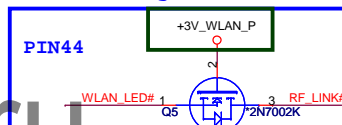
Support Wake Function(Reserve)



Mini Card Reset



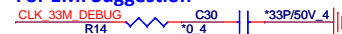
Avoid leakage issue



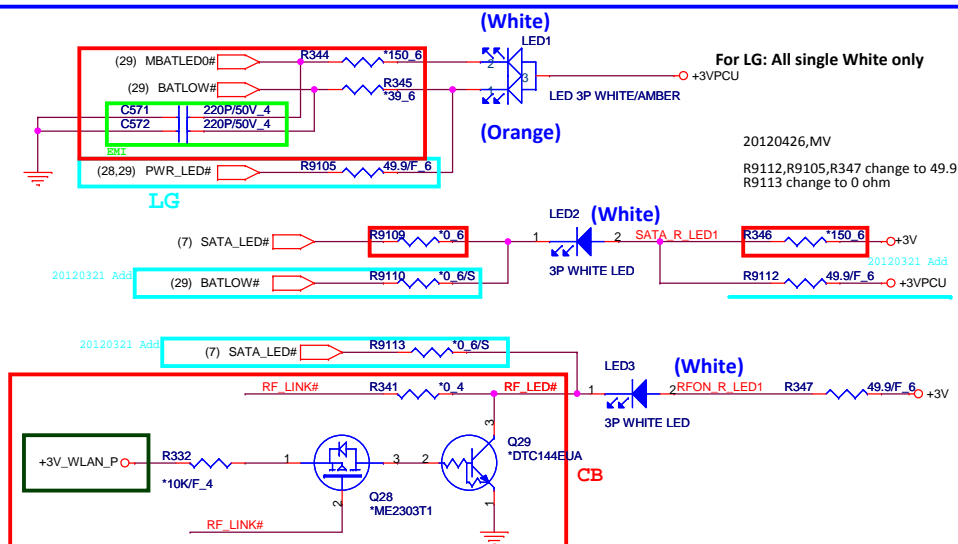
LGE mini-pcie power status

WLAN	Bluetooth	+3V_WLAN_1
Radio-ON	Radio-ON	Power-ON
Radio-ON	Radio-OFF	Power-ON
Radio-OFF	Radio-ON	Power-ON
Radio-OFF	Radio-OFF	Power-OFF

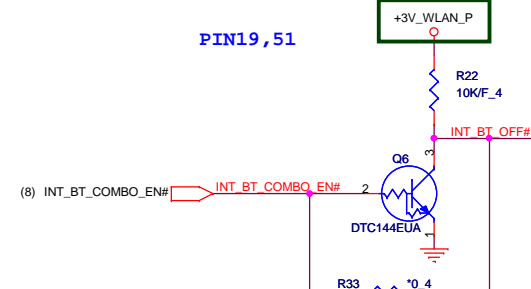
For EMI Suggestion



LED Status



PIN19,51

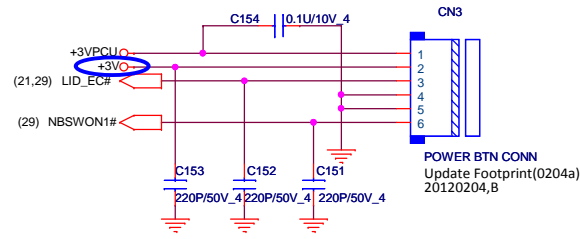


Left side Power Button Connector(1)

For CB

Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : +3V
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#

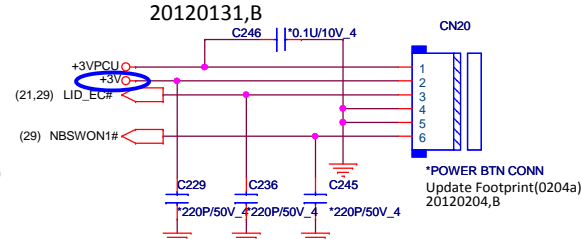
20120507,MV
Change CN3/CN20#2 to +3V



Right side Power Button Connector(2)

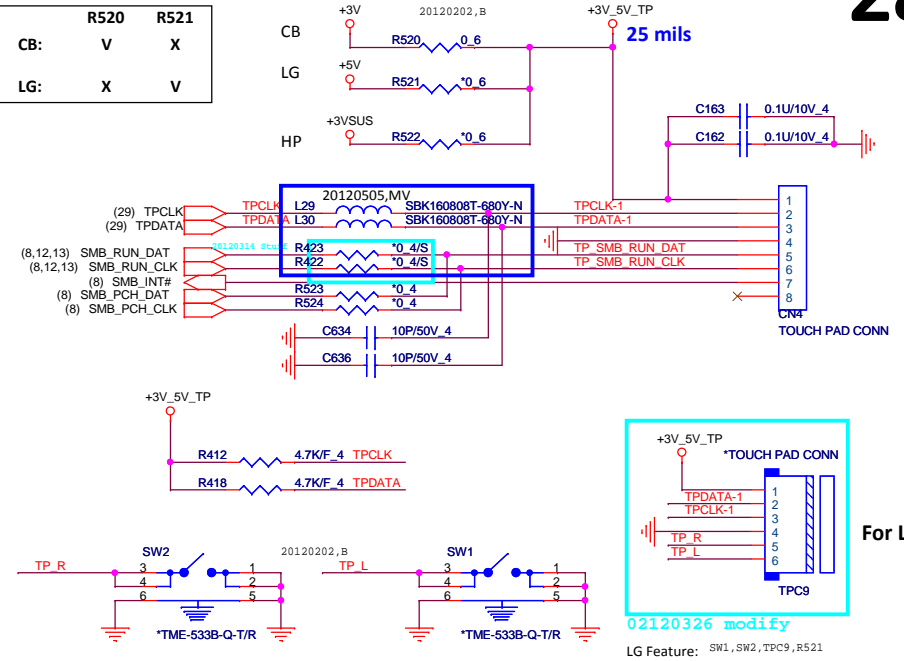
For LG

Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : +3V
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#

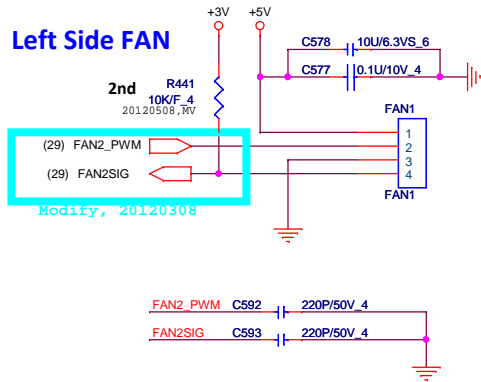


Touch Pad Connector

	R520	R521
CB:	V	X
LG:	X	V

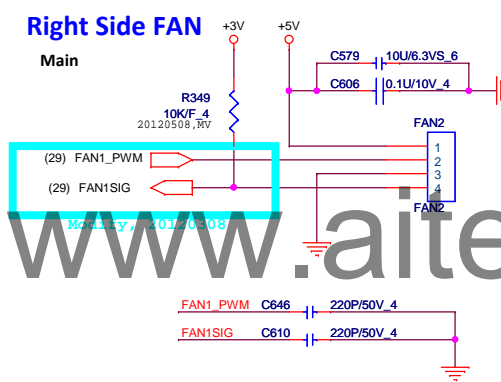


Left Side FAN

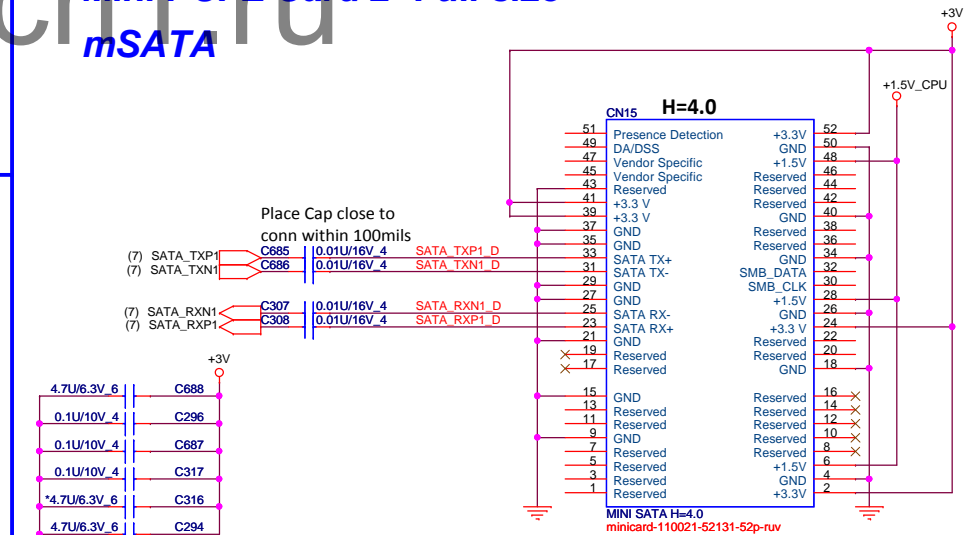


Right Side FAN

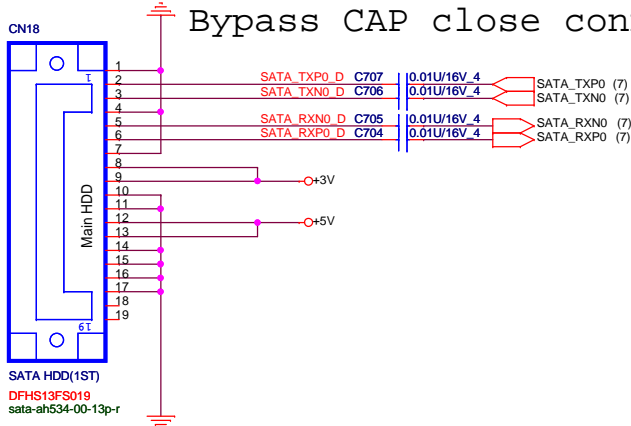
Main



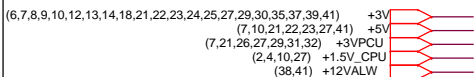
Mini PCI-E Card 2- Full size mSATA

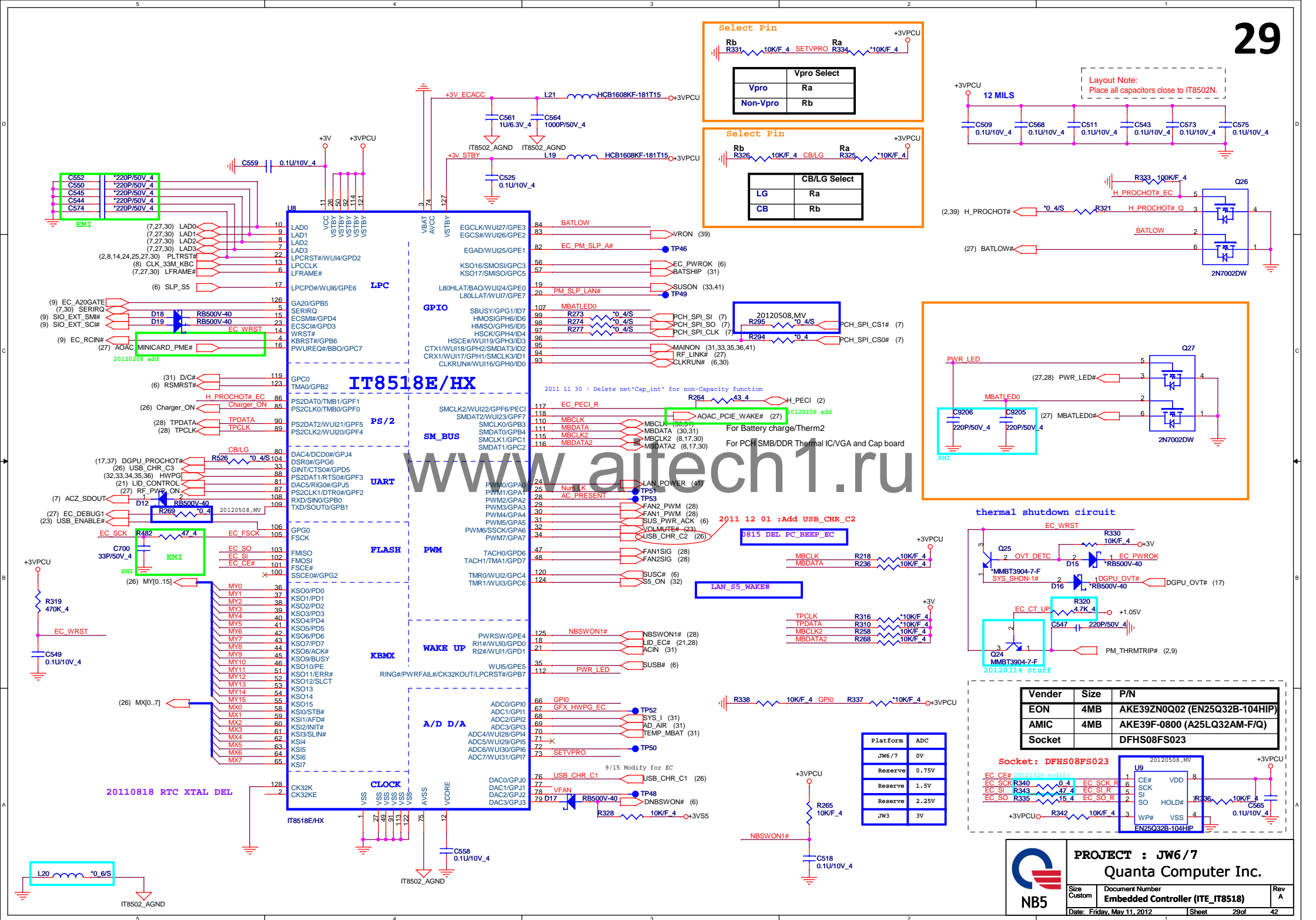


Bypass CAP close conn

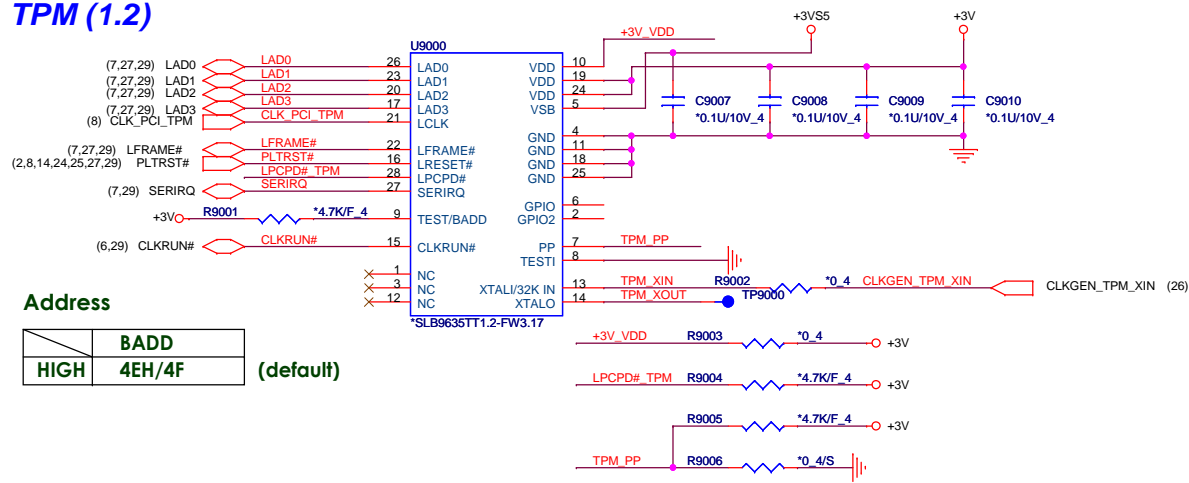


SATA HDD Connector(Cable type)

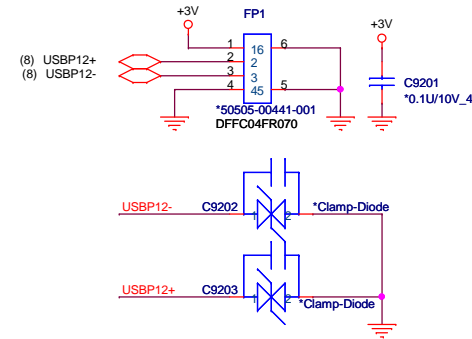




TPM (1.2)



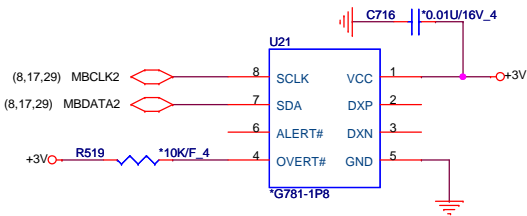
Finger Printer



Local Thermal Sensor

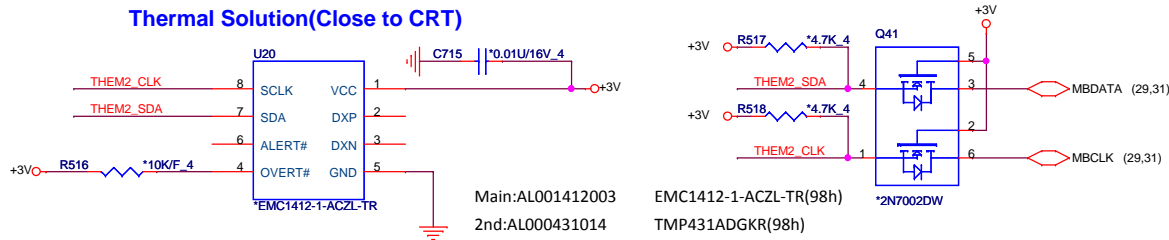
20120131,B

Thermal Solution(Close to GPU)

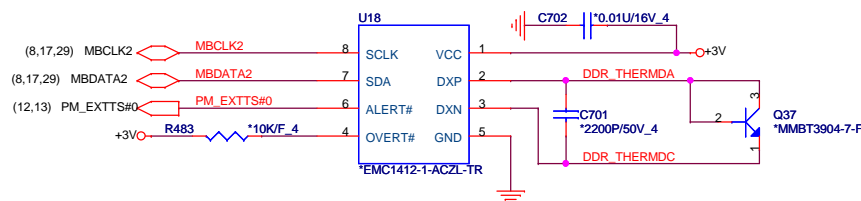


Main:AL000781039 G781-1P8(9Ah)
2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)

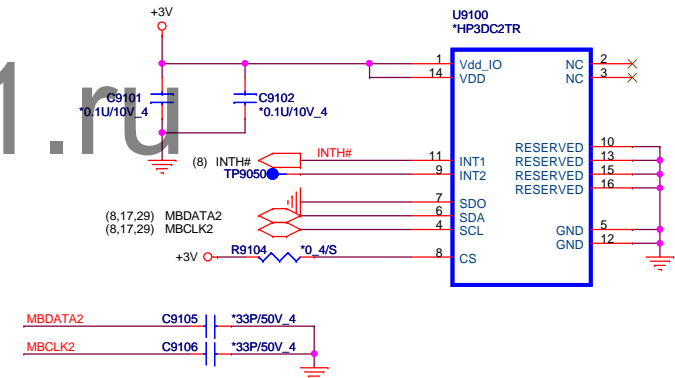
Thermal Solution(Close to CRT)



DDR3 Thermal Sensor



Accelerometer Sensor



SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low

I2C (ST HP3DC2) SDO,Pin7

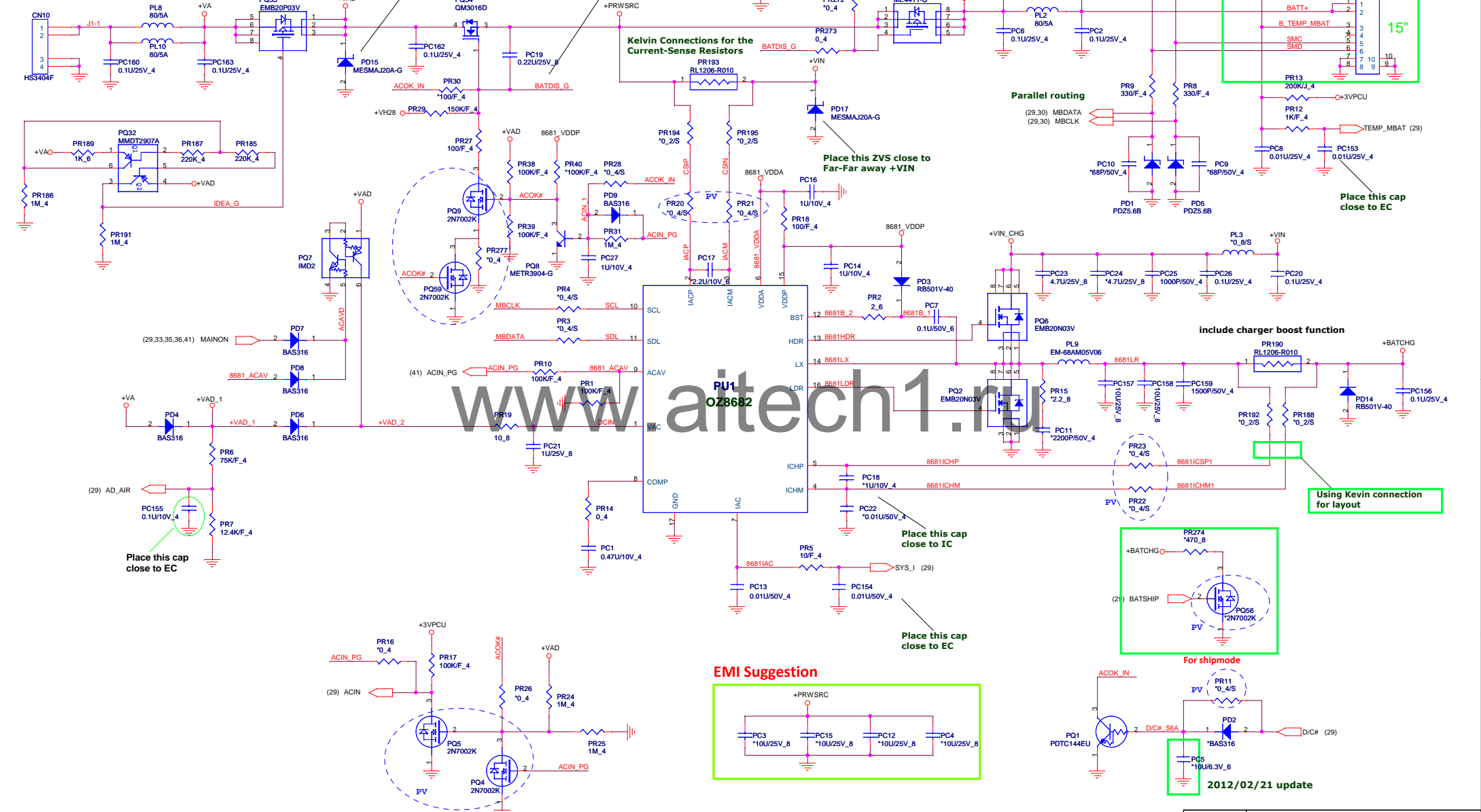
0x50	Gnd Default
0x52	VDD



PROJECT : JW6/7
Quanta Computer Inc.

Size Custom	Document Number G-sensor/FP/TPM/THEM	Rev A
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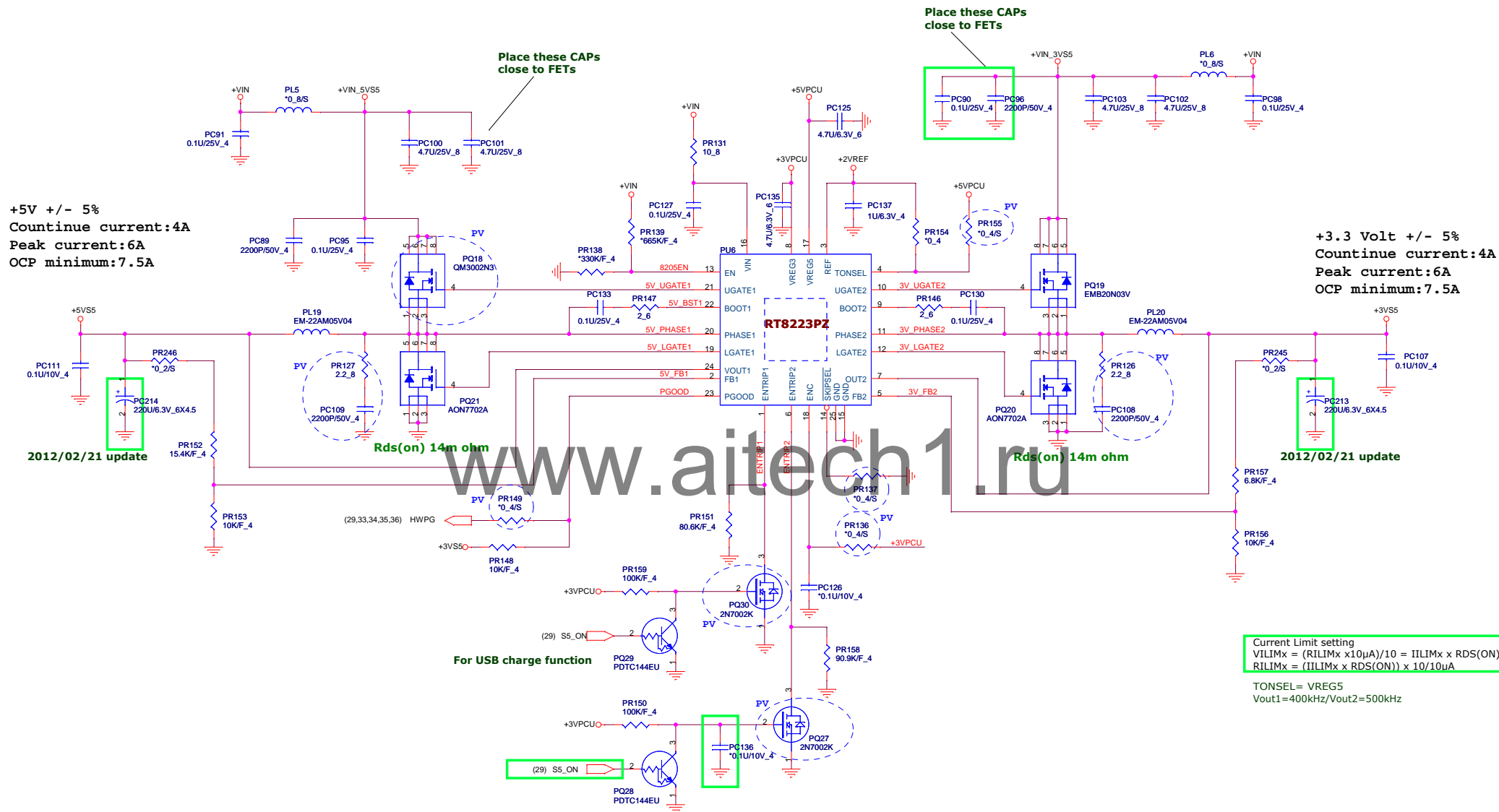
TOP DC_JACK
90W/4.75A



(21,32,33,35,37,38,40,41) +VIN
(41) +VAD
(41) +VH28
(41) +VAD₁
(7,21,26,27,28,29,32) +3VPCU

2012/02/21 update

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW



(21,31,33,35,37,38,40,41) +VIN
 (6,7,8,9,10,21,26,27,29,30,35,36,38,41) +3VSS
 (10,21,23,26,33,34,35,37,39,40,41) +5VSS
 (7,21,26,27,28,29,31) +3VPCU

NB5	PROJECT : JW6/7		
	Quanta Computer Inc.		
	Size Custom	Document Number 3/5VSS (RT8223P)	Rev A
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(VTT/2A)

(3mA)

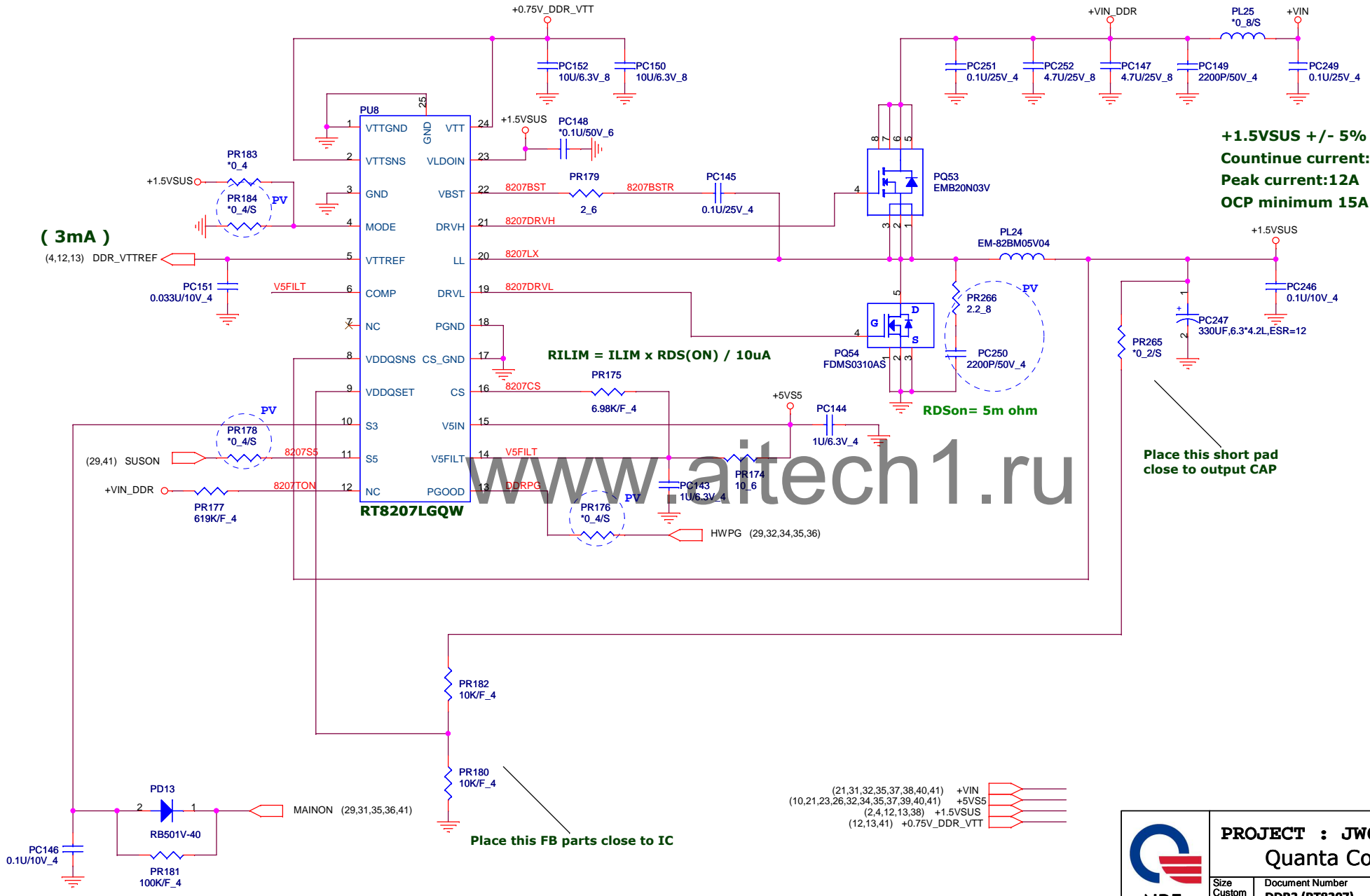
$$RILIM = ILIM \times RDS(ON) / 10\mu A$$

$RDSon = 5m\ ohm$

+1.5VSUS +/- 5%
Countinue current:6A
Peak current:12A
OCp minimum 15A

Place this short pad close to output CAP

Place this FB parts close to IC



- (21,31,32,35,37,38,40,41) +VIN
- (10,21,23,26,32,34,35,37,39,40,41) +5VS5
- (2,4,12,13,38) +1.5VSUS
- (12,13,41) +0.75V_DDR_VTT

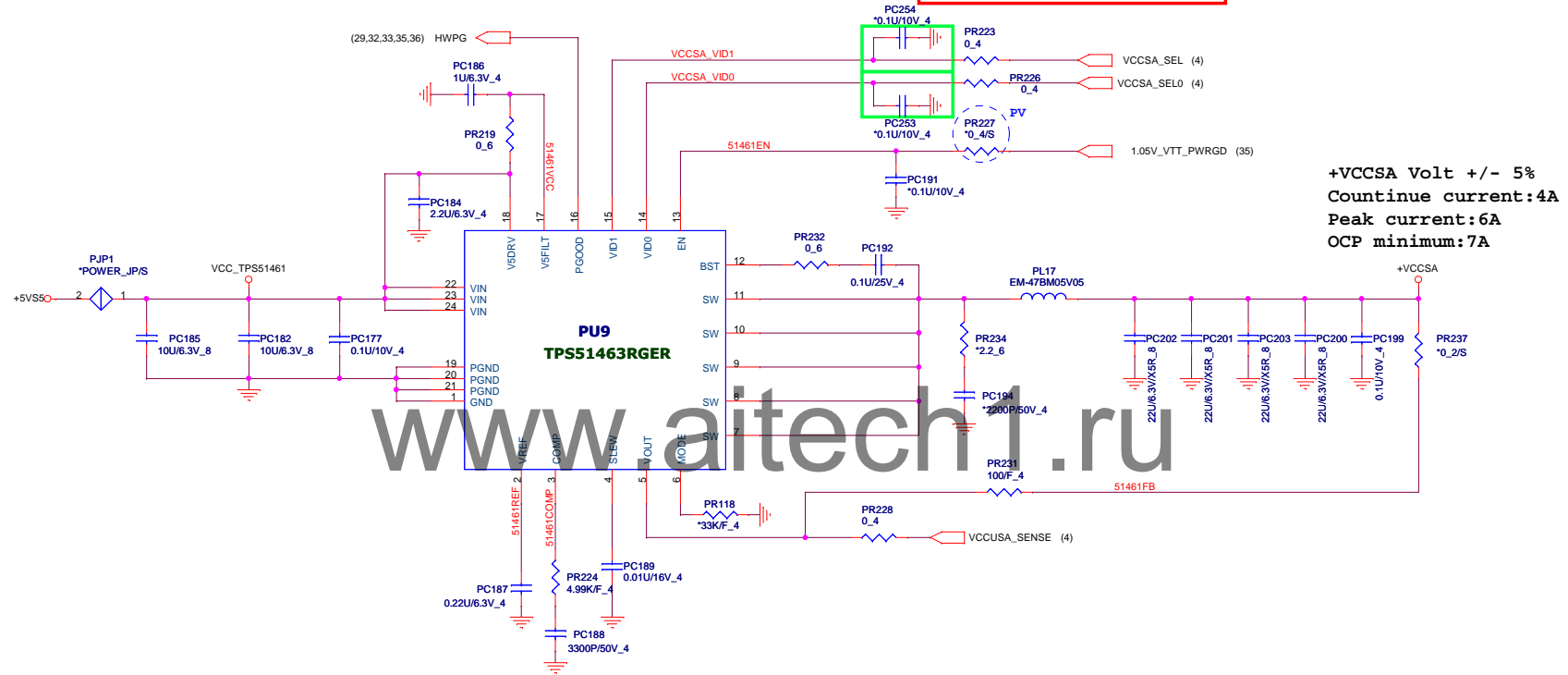
		PROJECT : JW6/7	
		Quanta Computer Inc.	
Size Custom	Document Number	Rev A	
	DDR3 (RT8207)		
Date: Friday, May 11, 2012	Sheet	33 of	42

ULV
1.7W

CPU system agent
voltage slew rate of 0.5 -10 mV/ μ s

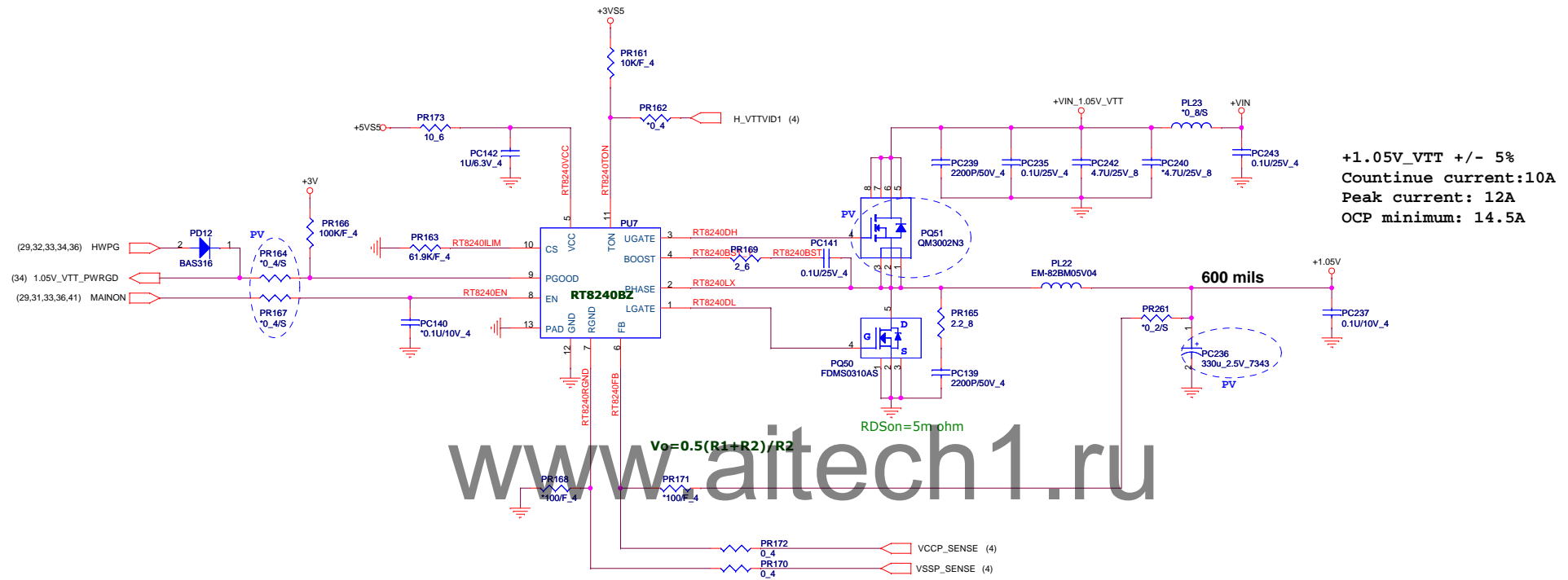
VCCSA	PU9
35W	TPS51462RGER
ULV 1.7W	TPS51463RGER

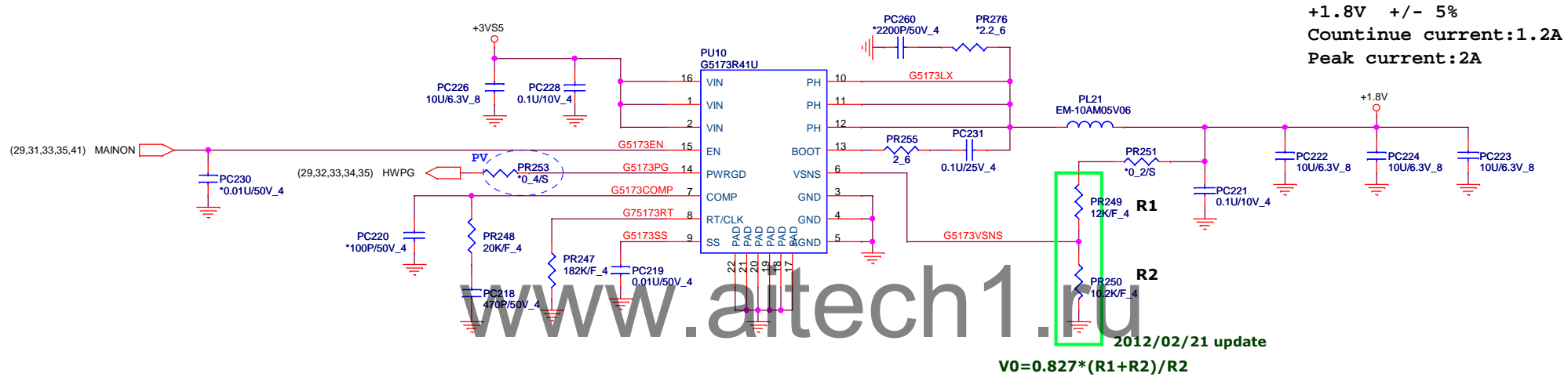
SELO	SEL1	+VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V



PROJECT : JW6/7
Quantia Computer Inc.

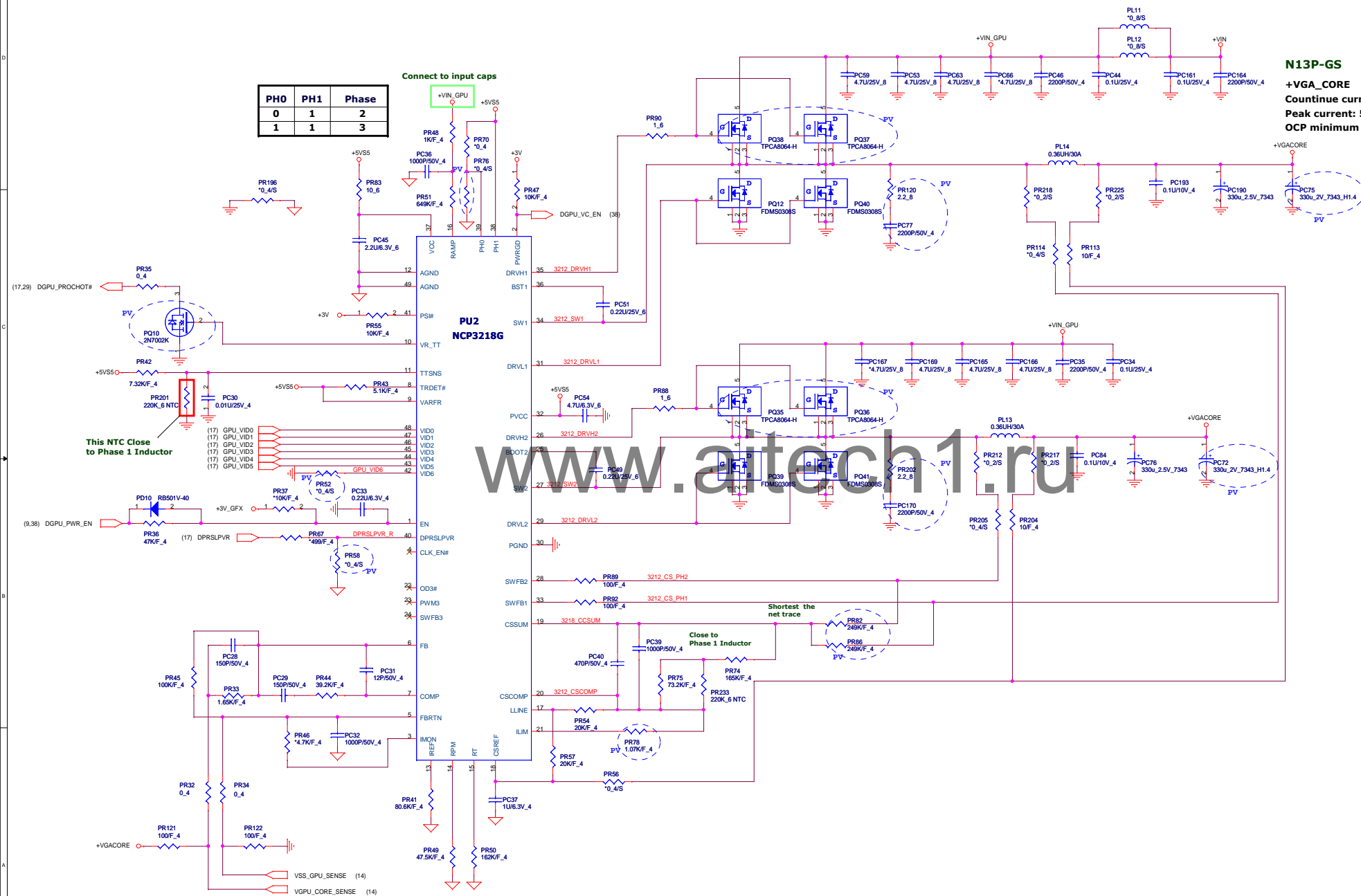
Size	Document Number	Rev
Custom	+VCCSA (TPS51462RGER)	A
Date: Friday, May 11, 2012	Sheet	34 of 42

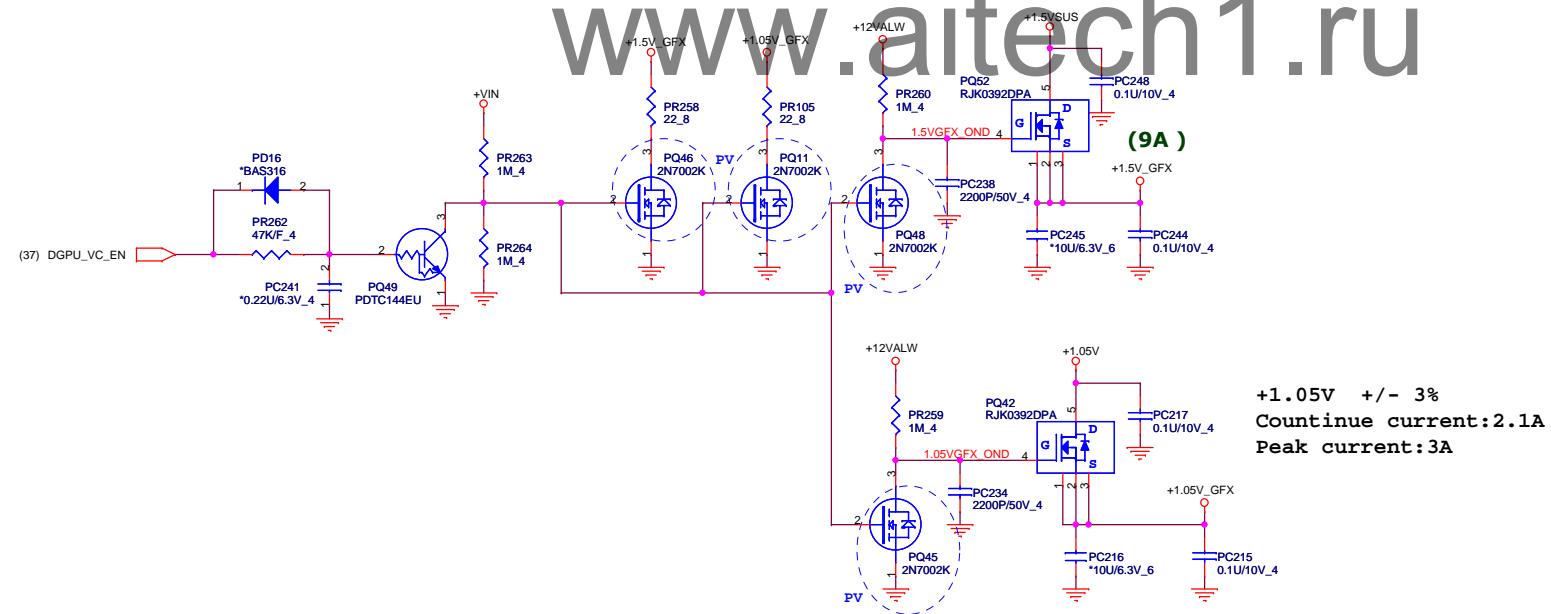


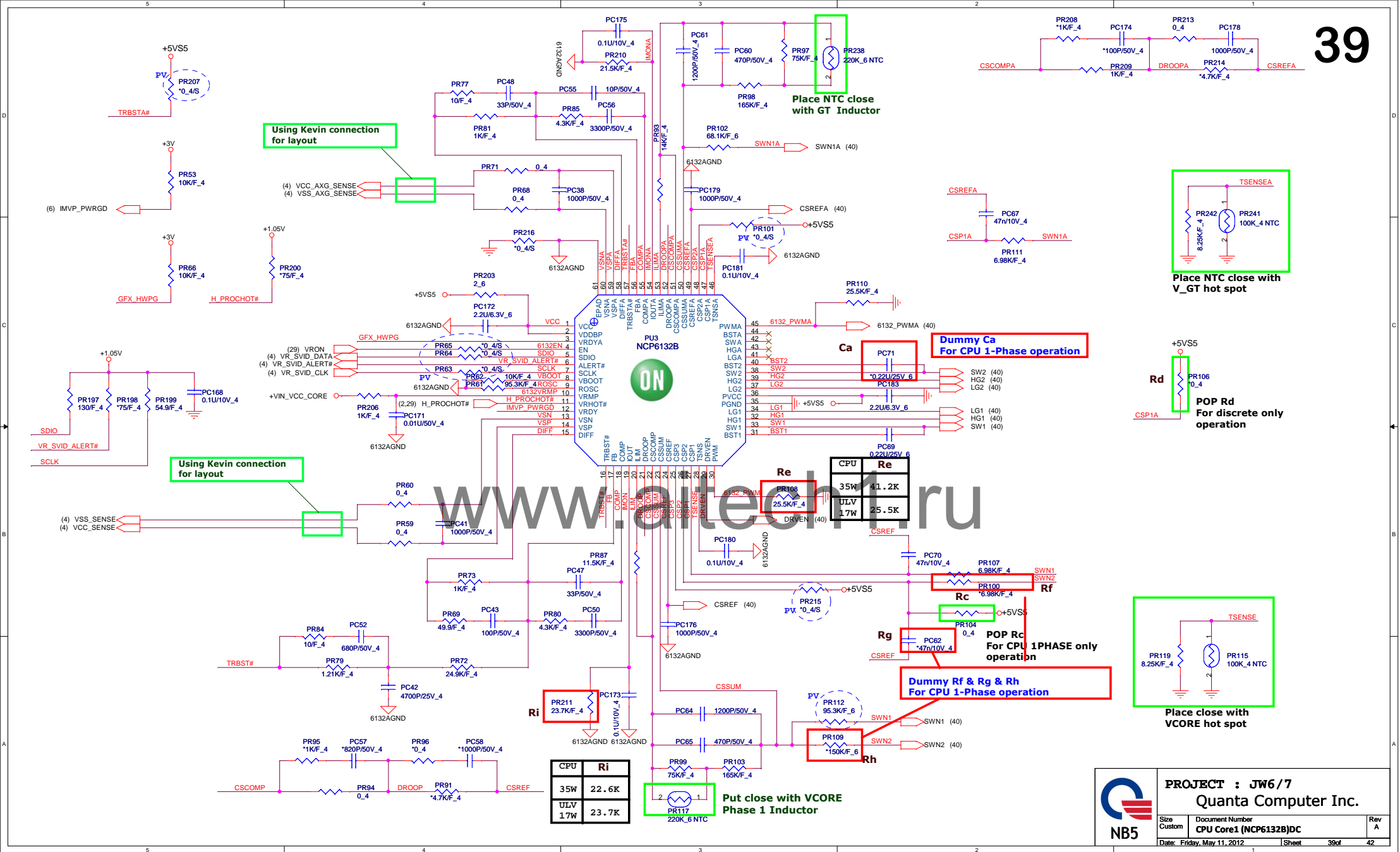


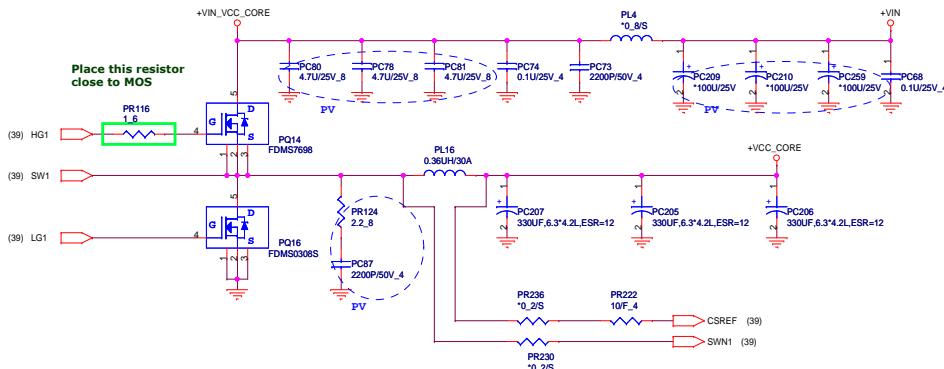
PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
B	+1.8V (G9661)	A
Date: Friday, May 11, 2012	Sheet	36of 42

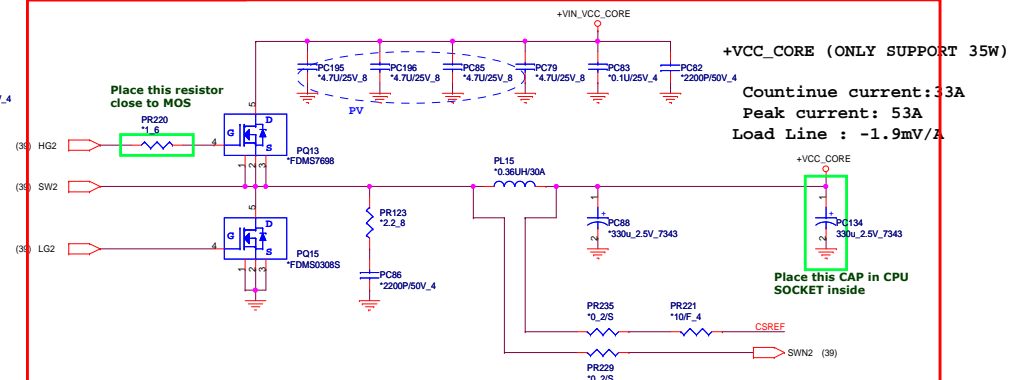








Dummy This Schematic
For CPU 1-Phase operation



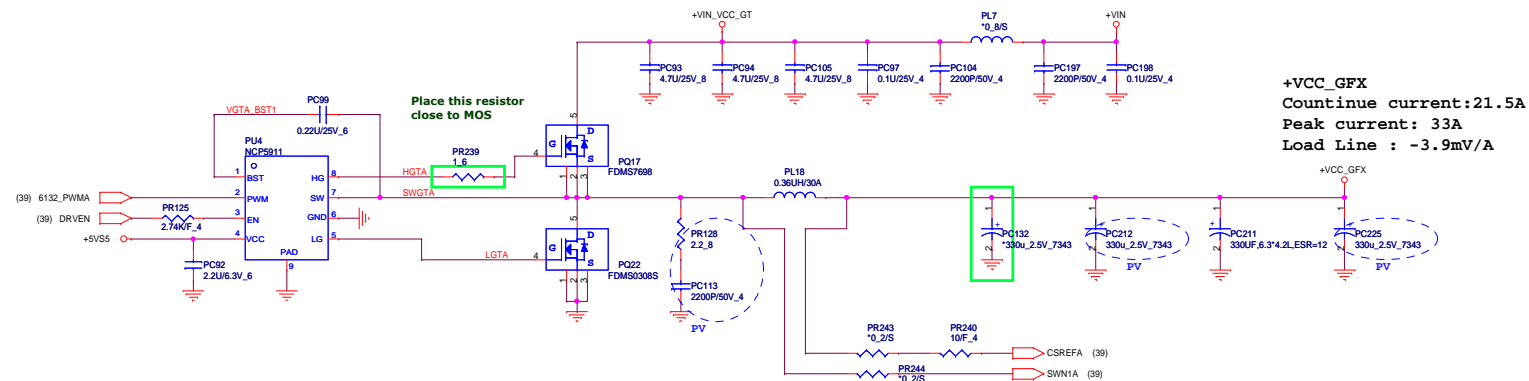
+VCC_CORE (ONLY SUPPORT 35W)

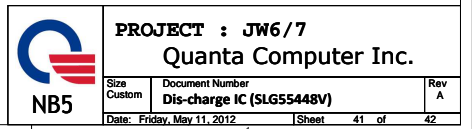
Countinue current: 33A
Peak current: 53A
Load Line : -1.9mV/A

+VCC_CORE (ULV 17W)

TDC : 25A
Peak current: 33A
Load Line : -2.9mV/A

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